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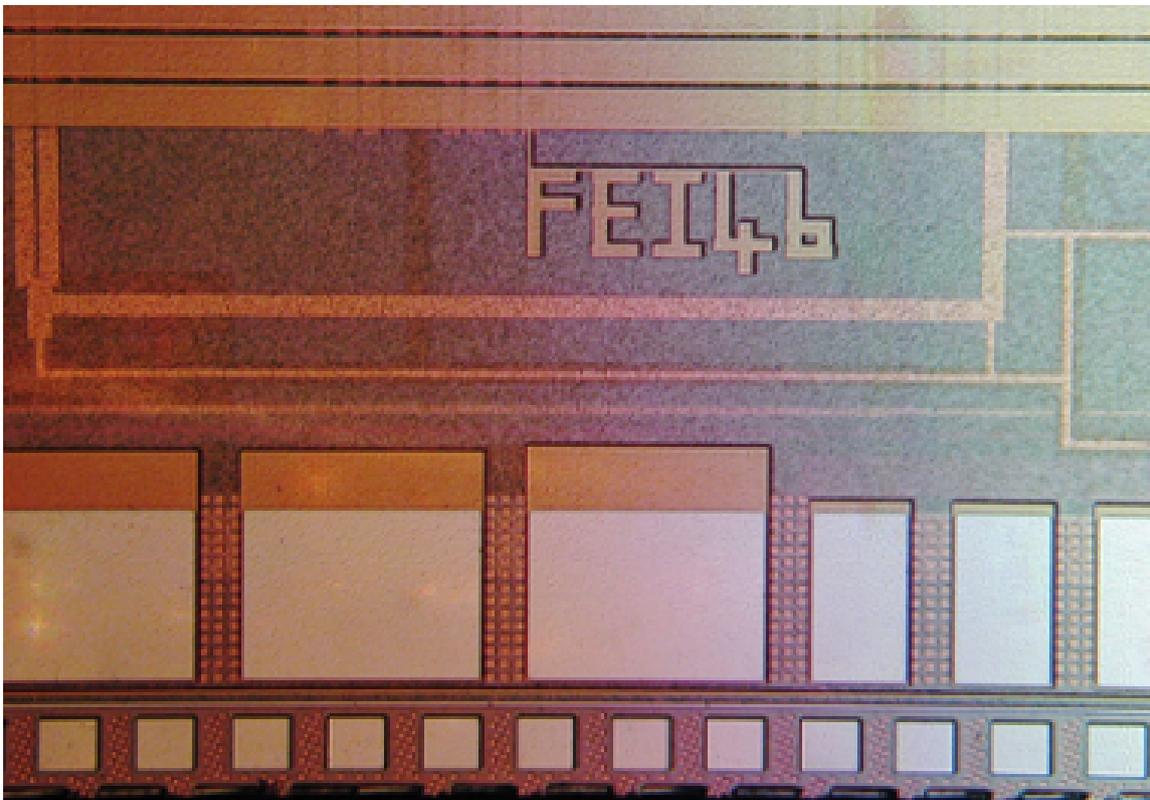
## The FE-I4B Integrated Circuit Guide

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### FE-I4 Collaboration

**ABSTRACT:** Detailed reference of the FE-I4 integrated circuit version B. Much of the text is the same as the FE-I4A guide, but register assignments, pads, etc. should be updated. early versions will not have all the needed updates.

**KEYWORDS:** ATLAS, LHC, sLHC, Upgrade, Pixel detector, Insertable B layer, CERN.



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## 1. Introduction

The FE-I4 integrated circuit contains readout circuitry for 26 880 hybrid pixels arranged in 80 columns on  $250\ \mu\text{m}$  pitch by 336 rows on  $50\ \mu\text{m}$  pitch. It is designed in a 130 nm feature size bulk CMOS process. The letter “B” in FE-I4B refers to the design revision intended for productoin of the Insertable B-Layer detector. The “B” will be generally omitted unless describing a specific feature of this version. Register assignments, pinouts, etc., in this document apply to FE-I4B and may be different in other versions. The main functional differences between FE-I4B and its predecessor, FE-I4A, are a redesign of the end of chip logic, the use of a specific power supply option, and the addition of some circuits that wre excluded from FE-I4A. A comprhensive list of changes is given in Appendix ??.

Sensors must be DC coupled to FE-I4 with negative charge collection. Each FE-I4 pixel contains an independent, free running amplification stage with adjustable shaping, followed by a discriminator with independently adjustable threshold. The chip keeps track of the firing time of each discriminator as well as the time over threshold (ToT) with 4-bit resolution, in counts of an externally supplied clock, nominally 40 MHz. Information from all discriminator firings is kept in the chip for a latency interval, programmable up to 255 cycles of the external clock. Within this latency interval, the information can be retrieved by supplying a trigger. The data output is serial over a current-balanced pair (similar to LVDS). The primary output mode is 8b/10b encoded with 160 Mb/s rate. The FE-I4 is controlled by a serial LVDS input synchronized by the external clock. No further I/O connections are required for regular operation, but several others are supported for testing.

The many details behind the simple introduction given above are collected in this document. Many of the specifications and features of FE-I4 have been derived from the FE-I3 chip used in the ATLAS pixel detector [4] and a familiarity with FE-I3 will be a useful point of reference to complement this document. This note is intended to both document the FE-I4 chip design and serve as a users’ guide for FE-I4B version operation. The reader interested in learning about the design should focus on sections 2–5 and ??, while the reader trying to operate the chip should focus on 3, 6–??, and the appendices.

300 **2. Specifications and Ratings**

The ratings given in this section are separated into power supply, temperature, and radiation. These are not recognized commercial or military ratings, but rather the results of ad-hoc tests, simulations, or estimates carried out to validate compatibility with design goals. It is assumed that further testing will be carried out to validate the use in each specific application, as needed.

Item	Value	Units
Pixel size	$50 \times 250$	$\mu\text{m}^2$
Bump pad opening diameter	12	$\mu\text{m}$
Input	DC-coupled -ve polarity	
Maximum charge	100,000	$e^-$
DC leakage current tolerance	100	nA
Pixel array size	$80 \times 336$	Col $\times$ Row
Last bump to physical chip edge on 3 sides	$\leq 100$	$\mu\text{m}$
Last bump to physical edge on bottom	$\leq 2.0$	mm
Normal pixel input capacitance range	100-500	fF
Edge pixels input capacitance range	150-700	fF
In-time threshold with 20 ns gate (400 pF) <sup>1</sup>	$\leq 4000$	$e^-$
Hit-trigger association resolution	25	ns
Same pixel two-hit discrimination (time)	400	ns
Single channel ENC sigma (400 fF)	$< 300$	$e^-$
Tuned threshold dispersion	$< 100$	$e^-$
Charge resolution	4	bits
ADC method	ToT	
Radiation tolerance (specs met at this dose)	300	Mrad
Operating temperature range	-40 to +60	$^\circ\text{C}$
Average hit rate with $< 1\%$ data loss	400	MHz/cm <sup>2</sup>
Readout initiation	Trigger command	
Max. number of consecutive triggers	16	
Trigger latency (max)	6.4	$\mu\text{s}$
Maximum sustained trigger rate	200	kHz
External clock input (nominal) <sup>2</sup>	40	MHz
Single serial command input (nominal) <sup>2</sup>	40	Mb/s
Single serial data output (nominal) <sup>2</sup>	160	Mb/s
Output data encoding	8b/10b	
I/O signals	LVDS	

1: At discriminator output. Digital hit detection in region will reduce sensitivity to time-walk.

2: Nominal operating frequencies. The design includes 20% frequency margin in general and  $\approx 100\%$  for the data output.

**Table 1:** Basic Specifications for FE-I4

305 **2.1 Specifications**

The specifications are listed in Table 1. In addition to these quantitative specifications, there are functional capabilities listed in Table 2 that “carry over” from FE-I3 to FE-I4. Additional features that represent new functionality are listed in Table 3.

<b>Capability</b>
Internal and external pulse calibration charge injection
Internal generation of all bias voltages and currents
SEU-tolerant, programmable global and pixel registers
Global discriminator OR output (“hitbus”)
Self-triggered operation mode based on hitbus
Analog test outputs for one or more pixels
Voltage regulators compatible with serial power
Individual pixel leakage current monitoring
Charge injector capacitor value measurement circuit
Power-on reset pins (require external capacitor to use)

**Table 2:** Capabilities “Inherited” from FE-I3

<b>Capability</b>
PLL clock multiplier to support high speed output from 40 MHz beam clock
Prompt radiation detector that automatically disables the chip
Two trigger modes: Continuous (single time-slice) and Stop (all time slices)
Programmable Read Only Memory in the form of e-fuses
Opposite-corner alignment marks for flip-chip pattern recognition
Isolated sensor connection through a chip bonding pad <sup>1</sup>
Internal error logging counters
10-bit ADC for monitoring
Temperature measurement circuit (using above ADC)
Programmable event size truncation

1: The isolation voltage of this connection is not rated and must be measured

**Table 3:** New capabilities in FE-I4B

## 2.2 Power Ratings and Start-up

310 The transistors used in FE-I4, even for I/O, have a 2.2 nm gate oxide normally reserved for core  
 circuitry. The chip voltage specifications are derived from the properties of this gate oxide. The  
 only exceptions are the EFUSE programming circuitry, and the power circuit inputs. For EFUSE  
 programming the thickest gate oxide for this process (5.2 nm) was used in order handle the pro-  
 gramming voltage. The input to voltage regulators and voltage reference circuit does not go directly  
 315 to any gate and is designed to tolerate 2.5V.

The maximum safe long-term operating voltage for a given oxide thickness is not simple to derive. It depends on temperature, desired lifetime (in 1000's of power-on hours or KPOH), gate area, and operating duty cycle. A 1 cm<sup>2</sup> gate area is rated for 1.6 V operation with a 1 PPM failure rate after 100 KPOH at temperature of 125°C. While this suggests that a large detector could operate 10 years at 1.6 V without failures, even before considering the lower operating temperature (which further extends lifetime), this value does not include any potential radiation effects. Therefore, we conservatively chose a 1.5 V maximum long term operation voltage as the FE-I4 rating.

An absolute maximum rating (a voltage never to be exceeded) is even more complex to determine. This is because permanent damage occurs long before a voltage high enough to cause instantaneous gate rupture is reached. A mechanical spring serves as a useful analogy. For a working spring, the thing one should not exceed is the elastic limit, which is reached long before there is any chance of breaking the spring wire. Transistor degradation mechanisms depend on temperature and area, but also on time spent at a given voltage. A long time above a relatively low voltage can cause more irreversible degradation than a short time at much higher voltage. In fact, there are recommended procedures for highly accelerated stress testing (HAST) burn-in that involve very high voltages (approaching 2.5 V across 2.2 nm oxide) for times of order 100 ns. Like the long term operating voltage, the FE-I4 absolute maximum ratings and transient voltages have been defined somewhat conservatively, by not relying on the added protection afforded by a low operating temperature.

The voltage ratings for FE-I4 are collected in Table 4. Also included in the table are estimates of the current consumption. A minimum operating voltage is provided to indicate that all chip circuits have been designed to operate correctly down to this level (but this is obviously not a safety limit). In the case of the voltage regulators the minimum voltage indicates that it should be possible to run the chip using this device at that input voltage. In FE-I4B the regulators outputs are *not* internally hard-wired to the internal power nets, in order to preserve testing and debugging flexibility. This choice was made because external wiring would be mandatory in any case, as the power distribution inside the chip is poor along the transverse direction (across the columns). Thus, FE-I4B can be operated in two modes, direct connection to the internal nets (as for FE-I4A), or through the voltage regulators as shown in Figure 1. The latter is the intended configuration for IBL, allowing the use of a single external supply voltage and also provides margin for use of resistive cables. The voltage regulators are inside the FE-I4 even though the figure shows them as separate blocks. Note that a reference voltage must be externally wired to each regulator. The FE-I4B provides two options for each analog and digital references, denominated “current reference” and “voltage reference” options.

The current reference option uses replica outputs from the master current reference and suitable internal resistors to produce two identical voltages that will result in 1.65 V regulated outputs under high resistance process corner and 2.0  $\mu$ A reference current. However, each reference has a “trim down” configuration register allowing the user to independently set them to any desired value below 1.65 V after startup. The current reference is powered from the analog regulator and a startup circuit ensures that the regulator functions as soon as power is applied. Since it is important for safety that the reference current be 2.0  $\mu$ A at startup (before any programming), the current reference trim bits have been implemented as wire bond pads. Thus calibration and bonding of these bits is necessary before using the regulators with the current reference option. This calibration can

be done by powering the chip directly, for example as part of the wafer probing.

360 The voltage reference option uses a true 2.5 V voltage reference powered from the analog regulator input (not output). This produces an analog reference resulting in 1.5 V analog regulator output and a digital reference resulting in 1.2 V digital regulator output. These voltages are not adjustable (except by using external resistors). The voltage reference is a new circuit in FE-I4B and must be tested before and after irradiation.

	<b>Internal Nodes</b>	<b>Linear Regulators</b>	<b>Units</b>
Min. operating voltage	1.20	1.40	V
Nominal operating voltage <sup>1</sup>	1.50	1.80	V
Max. operating voltage	1.50	2.50	V
Nominal current at zero occupancy	0.42	0.42	A
Min. current (no clock or config.)	0.05	≈0.2	A
Max. current at IBL occupancy	0.55	0.55	A
Peak transients allowed	1.75	2.50	V
Max. safe R/T cable resistance <sup>2</sup>	0.45	≈2	Ω

1: Assuming single power supply

2: This is the difference between max. and nominal operating voltage, divided by the change in current between max. and min. current.

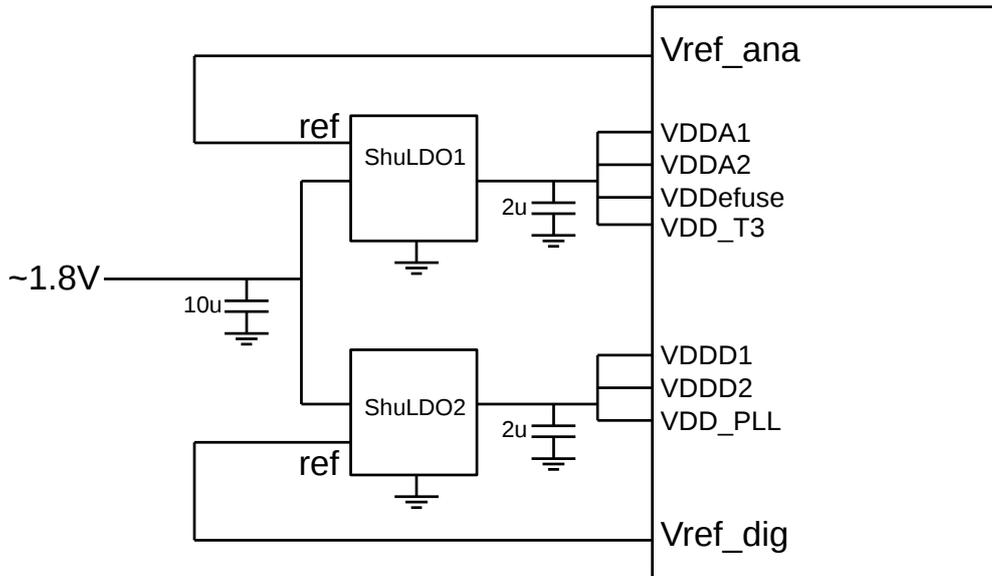
**Table 4:** Voltage Ratings and Current Consumption of FE-I4B

365 Internally, power is distributed by four main nets. Each net has separate wire bond pads for supply and for ground. In addition, the T3 isolation wells, the clock multiplier core, the EFUSE block, and the EFUSE programming voltage have dedicated power supply pins (but not separate ground). Table 5 lists what internal circuit blocks each net serves, and lists the relevant reset-bar pins. It also indicates which of the two regulators (Left or Right) should supply each internal  
370 net. The left ShuLDO is the designated analog regulator, while the right is the digital. All resets use negative logic. There is no internal power-on reset generation. Instead, pins are provided so that power-on resets can be implemented by adding external capacitors or tested with single ended signals as needed. The chip is forgiving of the powering sequence, with latch-up being very rare. When using the regulators all voltages will ramp up simultaneously.

### 375 2.3 Temperature Range

The FE-I4 has been designed to operate at low temperatures achievable with CO<sub>2</sub> cooling, as well as high temperatures for potential applications beyond silicon pixels. The recommended range where all specifications are met is -30°C to +30°C. However, the chip is designed to operate normally in the extended range -40°C to +60°C, but some specifications may not be met. Simulations to verify  
380 compliance with specifications have been carried out at -30°C, 0°C, and +30°C.

While operation anywhere in the allowed range is supported, some small temperature variation is present. On the digital side, power consumption is expected to vary over the given range. On the



**Figure 1:** Powering FE-I4B via the voltage regulators. The regulators are within the chip even though they are shown as separate blocks in the figure.

analog side, power consumption will remain constant, because it is tied to the current reference. No variation of the current reference has been observed in test devices with an accuracy of  $0.02\%/^{\circ}\text{C}$ .

385 A significant temperature variation exists in the discriminator threshold setting within the analog pixel, which is the sum of adding contributions from the DC level of the second stage and the replication of the global threshold voltage within the pixel. Each of these effects has been measured in prototypes to be approximately  $1\text{ mV}/^{\circ}\text{C}$ , but the exact values are expected to be process dependent. Making these circuits passively temperature compensated within the pixel would have  
 390 brought a significant area penalty and possibly also a significant power penalty. Instead, temperature compensation has been provided via the global threshold voltage generated in the bottom of chip (this is a single voltage distributed to all pixels). The global threshold voltage varies with temperature such as to mostly compensate the pixel temperature variation. Alternatively, a purely  
 395 external global threshold voltage can be supplied by overriding the internally generated voltage via a bonding pad.

## 2.4 Radiation Tolerance

The 130 nm feature size process used for FE-I4 enjoys an inherently high total dose radiation tolerance of the core (2.2 nm gate oxide) transistors. Design principles that take advantage of this benefit have been followed in order to exceed the 300 Mrad specification. Vulnerability to  
 400 single event upsets has been controlled by using custom layout, triple-redundant memory cells for storing configuration, triplicating digital logic blocs, and hamming coding data buses and storage. However, the FE-I4B is explicitly not robust against exposure to a very high dose rate source (note

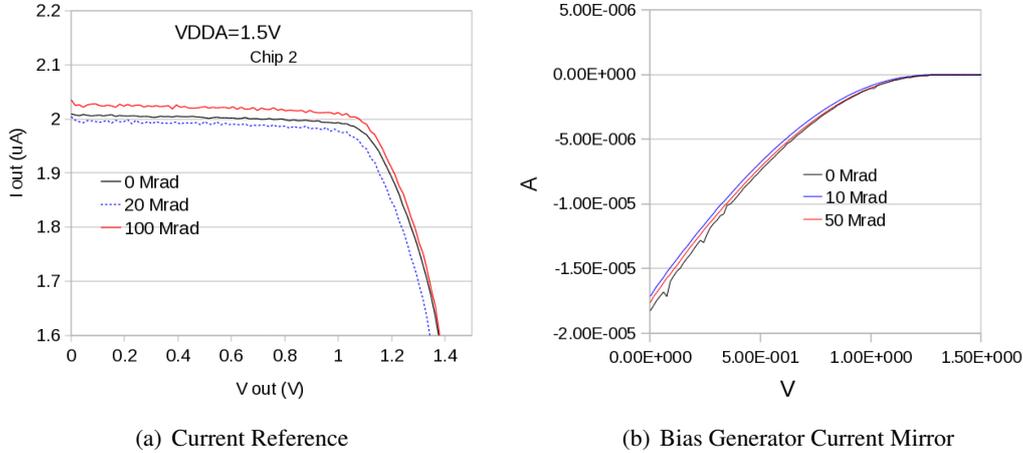
Net Name	ShuLDO	Reset	Internal Blocks Powered
VDDD1	R	RD1bar_P(88)	ESD protection for pads on this net RD2bar circuit Input LVDS receivers (with their own bias circuit) Command decoder IOMux bypass and test I/O block
VDDDT3_Pad <sup>1</sup>	L		T3 isolation wells
VDDA1	L	RA1bar_P(45) RA2bar_P(56)	ESD protection for pads on this net Current reference Radiation burst detectors Global configuration memory Bypass configuration memory Global bias DACs (but not bias mirrors)
VDD_PLL	R	-	Clock multiplier core ESD protection for this pad
VDDEfuse(42)	L	-	Core voltage EFUSE circuitry ESD protection for this pad
VDDD2	R	RD2bar_P(89)	ESD protection for pads on this net Digital columns and end of column logic Clock multiplier interface LVDS output End of chip logic All other digital circuits
VDDA2	L	-	ESD protection for pads on this net Bias generator mirrors Analog pixel array Pixel array shift register Pixel configuration latches all other analog circuits

1: The VDDDT3\_Pad net does not have added ESD protection because it consists entirely of substrate diodes, which are self-protecting.

**Table 5:** Power nets and blocks served, as well as which ShuLDO voltage regulator they should be supplied from. the ShuLDOs are identified as L(ef) and R(right). T Reset lines shown can be externally controlled if needed, either by logic or and R-C circuit, to implement power-on resets.

405 that high dose rate tolerance is not required for operation at particle colliders, where the integrated dose can be very high, but the rate at which the dose is delivered is always low). Dedicated radiation burst detection circuitry has been included in FE-I4B that will automatically reset the configuration memory in the presence of a dose rate exceeding  $10^8$  Rad/s. Such a rate must be present for 20 ns or longer in order to activate the reset. This was done to ensure that FE-I4B is not classified for export

control under ITAR. There are 3 redundant detectors (there were only 2 in FE-I4A) that must fire in coincidence in order to cause a reset. This is done to prevent accidental firings due to highly ionizing nuclear recoil events instead of high uniform dose rate (effectively single even upset of the radiation detectors).

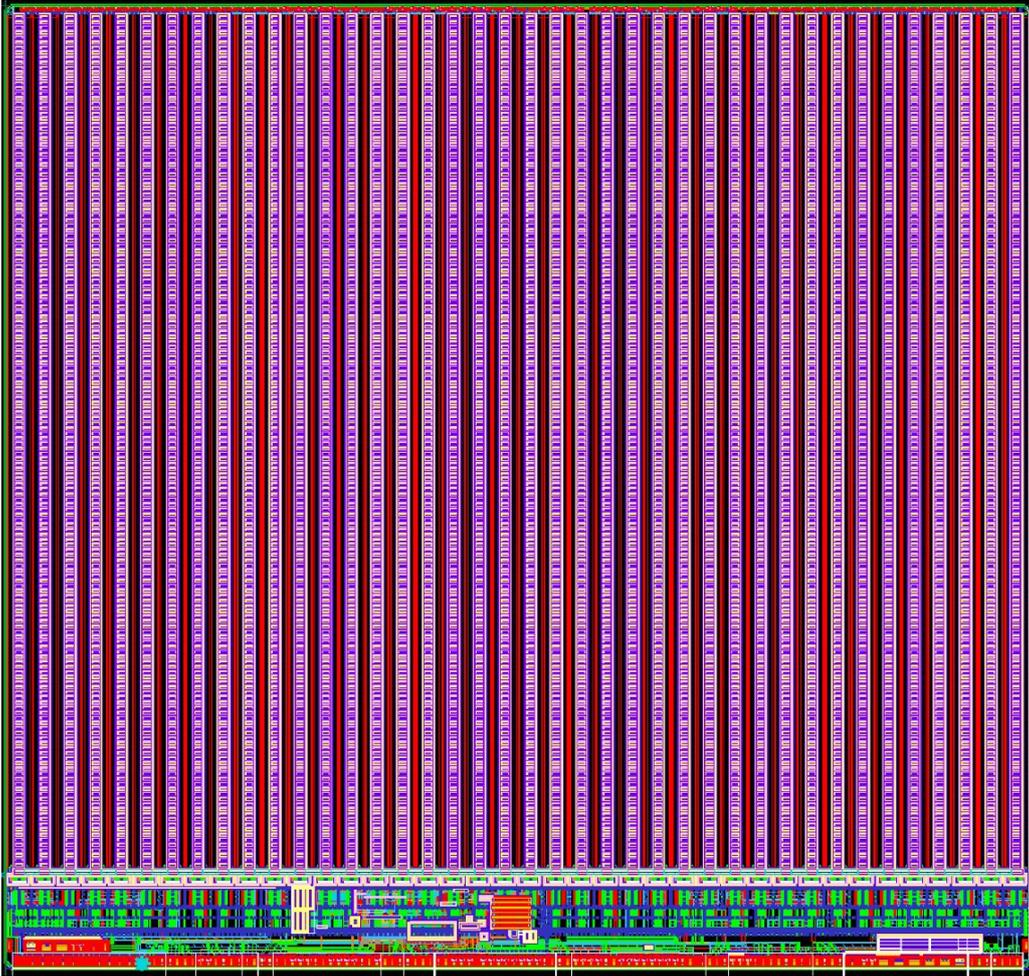


**Figure 2:** Radiation Effects on Prototype Circuits

Radiation tolerance has been measured with energetic protons, on small test chips during the initial FE-I4 development and later with full FE-I4A chips. Radiation tolerance of the chip itself is assessed by single chip irradiations (as opposed to modules with sensors), where the chip is under power and clocked during exposure and ionizing dosimetry is calibrated with aluminum foils. Measurements were made after 6 Mrad, around 300 Mrad, and at some intermediate points. The 6 Mrad point is important because that corresponds to the maximum threshold shift for the core transistors in this process.

Digital circuits showed no change after any of the above irradiations. Analog circuits have small, but measurable changes with dose. The current reference variation is about 2% over 200 Mrad (Figure 2(a)). The current mirrors used to generate bias voltages vary by about 5% (Figure 2(b)), but the same transistor configuration is used to turn the bias voltages into currents within each pixel, compensating for the change. Thus only small adjustment of the bias settings should be required after irradiation. The single pixel noise increase after irradiation is no greater than 10%. An exact figure is difficult to quote because noise measurements without a sensor are complicated by the lack of a proper load capacitance. Ultimately, prototype modules should be irradiated with chip power and clock to confirm the combined noise increase from both chip and sensor.

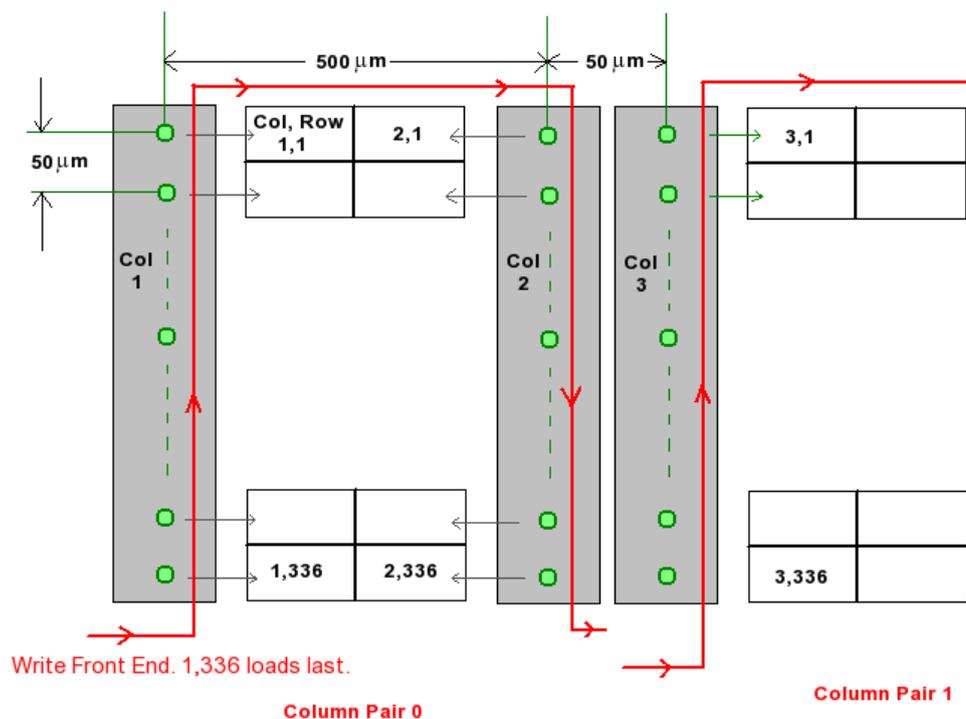
### 3. Layout and Organization



**Figure 3:** FE-I4 chip layout looking down onto the bump pads. The coordinate origin is at the bottom left corner, with x increasing to the right and y increasing upwards.

The FE-I4 layout is shown in Figure 3. References to the “top”, “bottom”, “left”, “right” of the chip are relative to this figure. The FE-I4A has no special identifying feature (logo). The pixel array has bump bond pads with  $12\ \mu\text{m}$  width octagonal openings on a  $50\ \mu\text{m}$  vertical pitch. In the horizontal direction there is one single column of bump pads along the left and right edges, with 39 pairs of columns in between, spaced  $500\ \mu\text{m}$  pair-to-pair, and  $50\ \mu\text{m}$  within each pair. The pads are aluminum. There are wire bonding pads along the bottom and top of FE-I4A. The pads at the top are specific to FE-I4A characterization and will not be present in a production version. The pads at the bottom come in three sizes, wide ( $250\ \mu\text{m}$  wide bonding area), normal ( $100\ \mu\text{m}$  wide bonding area), and narrow ( $75\ \mu\text{m}$  wide bonding area). Wide pads are exclusively for high current inputs and outputs and are intended for multiple wire bonds. Normal pads are for all other I/O that may be required for normal operation or that must be contacted during wafer probing. Narrow pads are for diagnostic only: they do not need to be contacted in wafer probing and will only be wire bonded

on an as needed basis to diagnose or correct problems or perform special measurements of chip internal voltages or currents. There is a short second row of pads on the left bottom of the chip, corresponding to a stand-alone linear-shunt voltage regulator. There are two normal pads further inset from the chip bottom, one each on the left and right edges, that make contact to isolated bump bond pads 50  $\mu\text{m}$  below the leftmost and rightmost full double columns of regular bump pads. Pads at the top of the chip are narrow pads oriented sideways. Note that the chip power nets all use multiple normal pads, instead of fewer wide pads, because power must be supplied uniformly along the width of the chip, and therefore the current in each power pad is small. Finally, the chip contains metal crosses for alignment during flip-chip assembly. There is one cross near each of the four corners, plus a half-cross near each of the lower left and right bump bond pads. Coordinates of wire bond pads and alignment marks are given in appendix F.



**Figure 4:** Pixel and column numbering scheme. The red line shows the pixel configuration shift register flow. Each double-column has an independent shift register. To program the pixels in columns 1 and 2 one must select double-column 0 for shift register programming, etc.

The FE-I4 pixel array is organized in column pairs numbered 0 (leftmost) to 39. A column pair consists of two analog columns, 336 pixels tall, on either side of a digital double column. The digital double column is actually a single column of 4-pixel regions, but it is called double column because it serves two columns of analog pixels. Single analog columns are numbered 1 to 80 (not 0 to 79). Thus column pair 0 contains columns 1 and 2. This can sometimes lead to confusion, but there is logic behind the choice. The pixel addressing scheme used for the output data is based on

single columns, and purposely avoided having a column address of 0 in order to exclude a unique all-0 data pattern. On the other hand, control of the chip is based on column pairs, not single  
460 columns, and in this case 0 was a desirable first address for simple decoding. The column pair,  
column, and row numbering convention is illustrated in Figure 4. The analog columns are shown  
in gray, with green circles representing the bump bonds to the sensor. The 4-pixel digital regions at  
the top and bottom of the digital double column are also shown. The pixel numbering is indicated  
as (column, row). Column 1 is along the left edge of the chip (recall there is no column 0). Row  
465 1 is at the top (there is similarly no row 0), and the first pixel (1, 1) is at the top left corner. Row  
and column addresses using this convention are always reported in the readout, along with the ToT  
value for the specified pixel *and* the pixel immediately below it in Figure 4. If there is only a hit in  
row 336 and not row 335 of a given column, the ToT for the “bottom” pixel is reported as “1111”,  
which is the ToT code for no hit. See Section 9 for more details on data output. See Section 7.2.2  
470 for details on how to select specific column pairs for control, calibration injection, etc. Pairing  
of columns for analog charge injection is anomalous due to layout constraints. Column “pair” 0  
controls charge injection only in column 1, column pair 1 injects into 2 and 3, column pair 2 into 4  
and 5, etc., and finally column “pair” 39 injects into the last 3 columns (see Section 7.2.2). This is  
the only addressing anomaly. All other operations that affect column pairs do so according to the  
475 standard convention of Fig. 4.

## 4. Circuit Core Description

### 4.1 Top Level Overview

A top level diagram of FE-I4 is shown in Figure 5. The FE-I4 pixel array is organized in double-columns like the present detector's FE-I3 chip, but the readout architecture is very different. Instead of moving all hits from the pixel array to a global shared memory structure for later trigger processing, the FE-I4 double-columns are further divided into  $2 \times 2$  pixel regions. Each region contains 4 identical analog pixels, ending in a discriminator, and one shared memory and logic block called Pixel Digital Region (PDR). The PDR can store up to 5 "events". For each event, a counter clocked at 40 MHz keeps track of the time elapsed since the event took place with 25 ns resolution. Clearly this requires distributing the 40 MHz clock to all the regions. The maximum skew of the clock distribution network is 2 ns. When an external trigger arrives, it is also distributed to all the regions simultaneously within 2 ns. The trigger selects any events for which the time counter matches the programmed trigger latency value. When the counter exceeds the latency without a trigger, the event is erased to make room for more. The events selected by a trigger remain in the region until it is their turn to be sent off chip via the serial LVDS output. The events are read out sequentially, ordered by time. All regions can be read out if they are all selected. A "stop" readout mode is also provided where the time counter is stopped and all events stored in every region are read out. This is useful for testing and debugging.

The individual discriminator outputs are synchronized with the 40MHz clock as they feed into the region logic, and all region operations are synchronous. Each synchronized discriminator output is further processed by applying a digital cut on the time over threshold (ToT). Hits smaller than a certain ToT (programmable between 1 and 3 clock periods) are classified as "small hits" and those larger as "large hits". The next available time counter in a given region starts whenever there is at least one large hit in the region. Small hits do not start a counter. Once a counter starts, a ToT code of all 4 pixels is always recorded (which is 1111 for a comparator that did not fire). This automatically stores small hits in the same time bin as large hits from the same cluster. This relaxes the time-walk requirements on the analog circuitry, allowing lower current operation. As clusters will often straddle a region boundary, in addition to storing all 4 pixels within the region, 4 neighbor bits are stored to flag the presence of small hits in the pixels adjacent to the region in the  $\phi$  direction. An association window of two clock cycles is used to capture small hits both within the region and in the 4 neighbor pixels. This scheme is equivalent to the hit duplication function of the FE-I3 chip, where all hits below a certain ToT value are copied to the preceding time bin, but it is more efficient in terms of memory and latency counter usage. Note that by setting the programmable digital ToT threshold to the minimum, one recovers traditional hit discrimination, in which all comparator firings are considered equal and recorded in the time bin that they occurred (which, due to time-walk, tends to be the wrong bin for hits just above the analog discriminator threshold).

All the above data driven information is stored locally in the 4-pixel digital region and only moved further if selected by a trigger. The raw hit rate that this architecture can accommodate with high efficiency is a function of the amount of memory in the region, and how quickly this memory is emptied (given by the programmed trigger latency). Events selected by a trigger potentially remain in the region much longer than the latency (until they are read out), and therefore a higher

trigger rate contributes to filling up the region memory, but because the trigger rate is low relative to the raw hit rate this is not a dominant effect. Figure 6 shows the simulated inefficiency for charge deposits in  $250\ \mu\text{m}$  planar unirradiated silicon at 3.7 cm radius of the FE-I4 as a function of the number of minimum bias interactions per 25 ns beam crossing, assuming a  $3750\ e^-$  discriminator threshold, 120 crossing latency, and 100 kHz trigger rate. The simulated performance of the present FE-I3 chip under the same conditions is also shown for comparison.

The FE-I4 inefficiency is dominated by single pixel pile-up, and not by the readout architecture, until well beyond the 75 interactions per crossing projected for IBL. The result can be applied to slightly different layer radius, the hit rate scales approximately as  $1/r^2$  [3]. In this simulation the rate of discriminator firing at 75 interactions per crossing was  $400\ \text{MHz}/\text{cm}^2$ . Single pixel pile-up, the main source of inefficiency, occurs when a pixel is hit while the discriminator is still high from a previous hit. This source of inefficiency scales linearly with the average ToT for a hit pixel and with the pixel area. The requirement to keep the total inefficiency below 1% was the driving reason for reducing the FE-I4 pixel area (relative to FE-I3) as well as the ToT dynamic range to 4 bits instead of 8.

The FE-I4 circuitry is divided into functional blocks with well-defined interfaces. This facilitated the design process carried out by a geographically distributed collaboration. Figure 7 shows a simplified schematic of the data path in a typical data acquisition configuration, while Figure 8 shows the simplified command and configuration path for single chip operation.

It may be appreciated from these figures that the output path is common for data and configuration, which both use a common fixed format record as detailed in Section 9. In terms of physical area, 89% is taken up by the 40 double-columns, each consisting of two analog columns and a Digital Double-Column (DDC). These are interfaced to the global control and logic on the chip periphery by a “horizontal” circuit layer running along the bottom of all columns and containing the end of digital column logic (EODCL in Figure 7) and the distribution of analog column configuration, bias, and calibration signals (Figure 8). All the periphery circuit blocks are single double-column oriented, with data, clocks, biases, etc. distributed to/from one or more double-columns in parallel as programmed into the global configuration. Many functions of the periphery logic blocks are programmable, and the global configuration is implemented as a random access memory of 16-bit words. For example, the clock source used to serialize output data can be selected to be any of the PLL outputs (40 MHz, 80 MHz, 160 MHz, or 320 MHz), the raw 40 MHz input clock, or an auxiliary input. The data output block can be configured to implement 8b/10b encoding or not, or to loop back the input clock, and so on. The configuration memory is implemented with triple-redundant SEU hard custom cells, while the digital logic blocks are either triplicated with majority voting or Hamming coded, always synthesized from standard cell libraries.

The main circuit block acronyms are summarized in Table 6. They are described in the following sections highlighting design and performance features. Practical details for operation (what value to program into which register, what wire bond pad to connect, etc.) are not given circuit-by-circuit in this chapter, but are collected for the chip as a whole in the appendix.

## 4.2 Analog Pixel

A 2-stage amplifier configuration is used to implement the analog front end, shown schematically in Fig. 9. The “Preamp” (first stage) is a cascode amplifier with an NMOS as input device. The

Acronym	Name	Contained in
FEND	Analog pixel (Front END)	analog column
CREF	Curent Reference	
VREF	Voltage Reference	
BIASDACS	BIAS generator using Digital to Analog Converters	
PDR	Pixel Digital Region	DDC
DDC	Digital Double Column	
EODCL	End Of Double Column Logic	
CMD	Command Decoder	
EOCHL	End Of Chip Logic	
DOB	Data Output Block	
PLL	Phase Locked Loop clock multiplier	CLKGEN
CLKGEN	CLocK GENERator	
CNFGMEM	CoNFiGuration MEMory	
EFUSE	PROM configuration using E-fuses	
PULSGEN	PULSe GENERator (for calibration)	
GADC	Generic ADC	
TEMP	Temperature Sensor	GADC
SHULDO	Shunt-LDO voltage regulators	

**Table 6:** List of Main Circuit Blocks

560 second stage (“Amp2”), AC coupled to the preamp, is a folded cascode PMOS input amplifier. The main motivation of this 2-stage system is to provide enough gain in front of the discriminator while permitting optimization in the choice of the preamp feedback capacitor ( $C_{f1}$ ). The discriminator is built with a 2-input voltage comparator and a threshold voltage generator. Signal shaping is only done by the preamp with an adjustable return to baseline, while the second stage provides only

565 voltage gain (given by  $C_1/C_{f2}$ ). The return to baseline and discriminator threshold are individually adjustable in each pixel, with globally determined range and offset. Altogether 13 bits are available for the configuration of the analog pixel which are stored locally in custom-made SEU-tolerant latches. Two selectable capacitors are provided for analog calibration injection. The preamp feedback has a low frequency active filter for DC leakage current compensation, and the amount of DC

570 leakage is mirrored to a column-parallel output. The comparator output is fed to the digital pixel region through logic gates which allow to gate it off or combine (logic OR) with a digital test signal. Additionally the comparator output is fed to column-parallel wired-OR circuit. This "HitOR" function can be disabled and should be off for normal operation to avoid parasitic crosstalk.

When a negative charge (electrons)  $Q_{in}$  is deposited at the input, a positive going pulse appears

575 at the output of the preamp. In an ideal system, the amplitude of this pulse would be  $Q_{in}/C_{f1}$ , but because a fast shaping (return to baseline) is required and the amplifier is non-ideal in practice, the actual amplitude will be less. The shorter the (adjustable) shaping, the smaller the pulse amplitude for the same input charge. The return to baseline is implemented by a feedback system very similar

to that of the FE-I3, discharging  $C_{f1}$  with a quasi-constant current source. The negative going pulse  
 580 at the output of the second stage feeds the negative input of the comparator, with a threshold voltage  
 at the positive input.

The schematic of the leakage current compensated preamp is shown in Fig. 10. It is a regulated  
 telescopic cascode with the NMOS input transistor M1. The availability of triple-well structures  
 allows to exploit the higher transconductance of NMOS transistors with respect to PMOS and  
 585 still be shielded from substrate noise. In addition, the NMOS input transistor gives a low DC  
 output potential that introduces a high dynamic range for the expected positive going output signals.  
 Due to the regulated cascode formed by the cascode transistor M2 and the amplifier composed of  
 transistors M5, M6 and M7 the preamplifier has a high output impedance and hence a high gain.  
 Since the biasing voltage of the cascode transistor M2 is generated locally the amount of potential  
 590 crosstalk paths are reduced and global routing is simplified. Transistor M4 provides additional  
 current to the input transistor M1, to increase its transconductance. The telescopic structure has  
 the advantage that the highest current in the amplifier flows through the input transistor and not  
 through any biasing transistor which reduces the noise contribution from the biasing. The source-  
 follower formed by transistors M8 and M9 decreases the output impedance in order to drive the  
 595 load presented by the coupling capacitor to the second stage without reducing the bandwidth.

\*\*\* ABDER: can you modify/add some explanation of what is it that allows operation down to  
 very low current? \*\*\*\*\*

The NMOS feedback transistor M18 providing continuous reset is biased in a current mirror  
 topology.

600 \*\*\*\* ABDER, CAN YOU REWRITE THIS NEXT BIT? IT IS NOT CLEAR. IT SHOULD MEN-  
 TION M20 \*\*\*\*\*

The bias current flows into the source-follower at the preamp output, but this does not affect the op-  
 erating point because it is much smaller than the bias current of the source-follower. The feedback  
 bias current is defined by a global PMOS biasing voltage. The feedback bias current can be tuned  
 605 at pixel level by a local DAC which steers a current into the gate-drain biasing transistor M19.

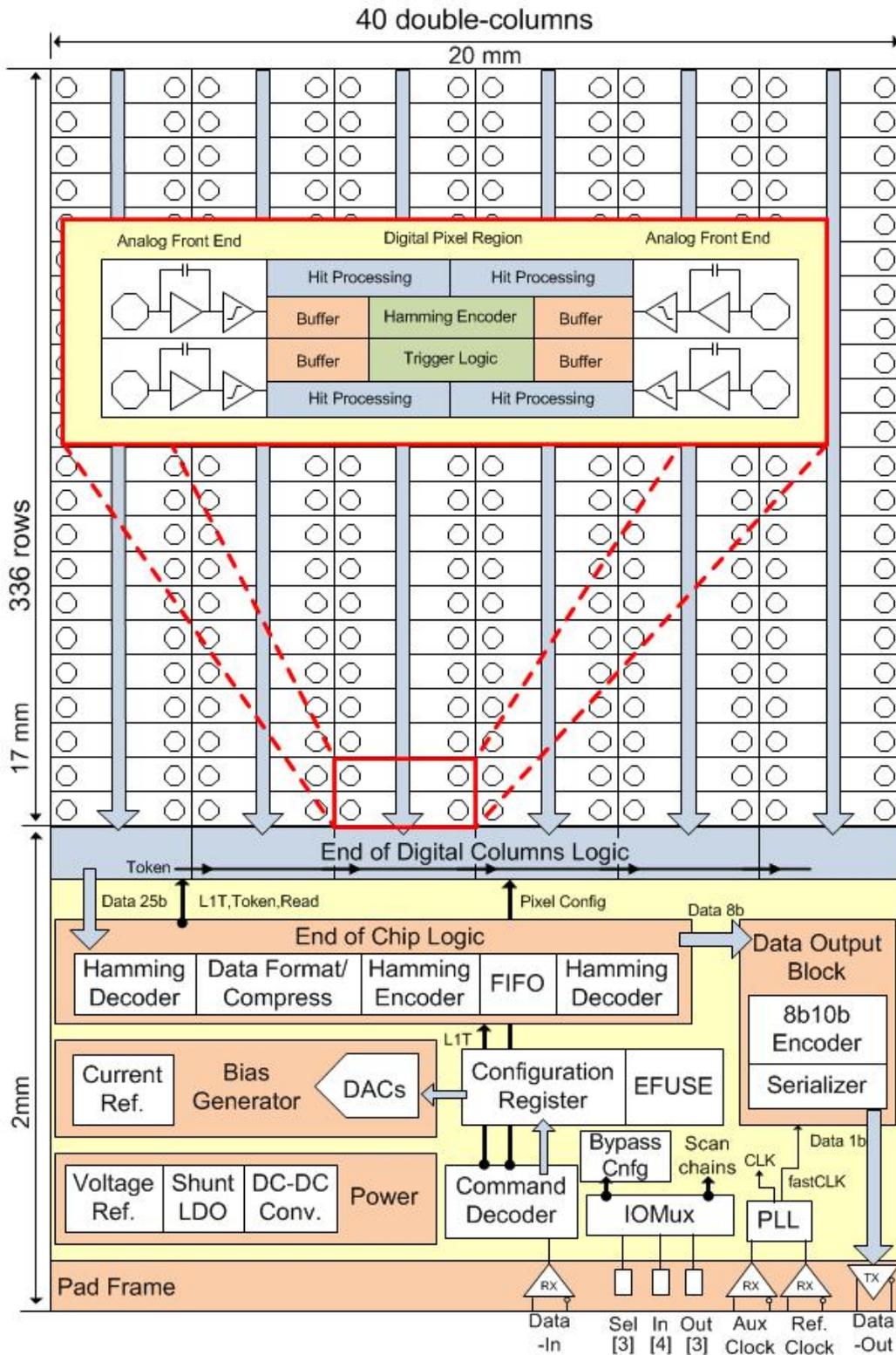
For high output signals, the NMOS feedback transistor M18 gets saturated and drains a constant  
 current. A nearly linear return to baseline and as a result a pulse width proportional to the input  
 charge is obtained. During the response to an electron signal, the potential at the preamp output  
 is higher than the potential at the input. As a result the terminal of transistor M18 which is con-  
 610 nected to the preamp input becomes the source which stays at constant potential. On the contrary,  
 the source of the gate-drain connected feedback bias transistor M19 is located at the output and  
 the source potential follows the output signal. To avoid that the feedback current changes with  
 the preamp output voltage the gate potential of the feedback transistor is stabilized by means of  
 capacitor  $C_1$ .

615 A differential amplifier (transistors M11-M15) tracks the DC shift between input and output of  
 the preamplifier, which is caused by detector leakage current. The dedicated PMOS transistor M15  
 connected to the preamp input is steered to compensate for DC leakage current. The bandwidth of  
 the differential amplifier has been limited by the addition of the capacitor C2 connected to the gate  
 of M15. As a result the differential amplifier reacts very slowly to voltage variations at the output  
 620 and so is insensitive to AC signals. The leakage current is mirrored to transistor M16 and can be  
 monitored when transistor M17 is switched on.

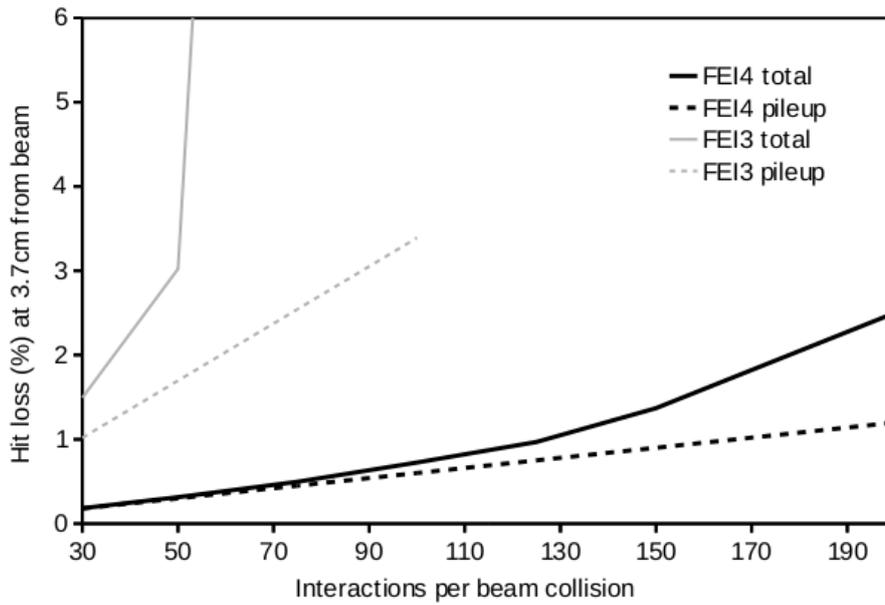
The second stage is shown in Fig. 11 together with the com- discriminator. A PMOS input transistor has been chosen for the cascode to give a large dynamic range for the expected negative going output signal. The bias voltage of the cascode transistor M3 is generated locally to ease routing. The feedback time constant of the second stage has been chosen to be significantly larger than the feedback time constant of the first stage. In this way a signal undershoot below the DC potential at the output of the second stage is avoided. The PMOS feedback transistor M10 is only used to set the DC operating point at the second stage input. During signal processing almost no discharge of the feedback capacitor happens through the PMOS feedback transistor. The feedback capacitance is charged and discharged only through the coupling capacitor  $C_C$  which connects the output of the first stage to the input of the second stage.

The comparator uses a classical two-stage differential amplifier, where the inverting input corresponding to the gate of transistor M12 is connected to the second stage output and the non-inverting input corresponding to the gate of transistor M13 is connected to a trimmed DC voltage which is provided by the local threshold tuning system. The second comparator stage is powered by the digital supply voltage to avoid that the current transients which are generated by the comparator switching couple to one of the amplification stages through the supply lines. The global threshold  $V_{thGlobal}$  is applied to the input of a source-follower which is formed by transistors M18, M19 and M20. A local voltage offset is added by the threshold tuning DAC (TDAC) formed by the resistor ladder and the current source M19. In addition to the TDAC offset, the source-follower adds a natural voltage-offset to  $V_{thGlobal}$  which corresponds to the source-gate voltage of transistor M18 and is defined by the current provided by transistors M19 and M20. Since the current provided by M19 is adjustable to define the LSB of the TDAC, most of the current should be provided by M20 to make the source follower offset independent of TDAC LSB. M20 has been biased with the second stage bias  $V_{bp}$  in order to save a bias line, as the exact value of the M20 current is not important. This source follower is TDAC circuit is very compact but has a known temperature dependence coming mostly from the has a known temperature dependence in the natural offset of the source follower. The approach taken to correct this temperature dependence is to introduce a compensating temperature dependence into the generation of  $V_{thGlobal}$ .

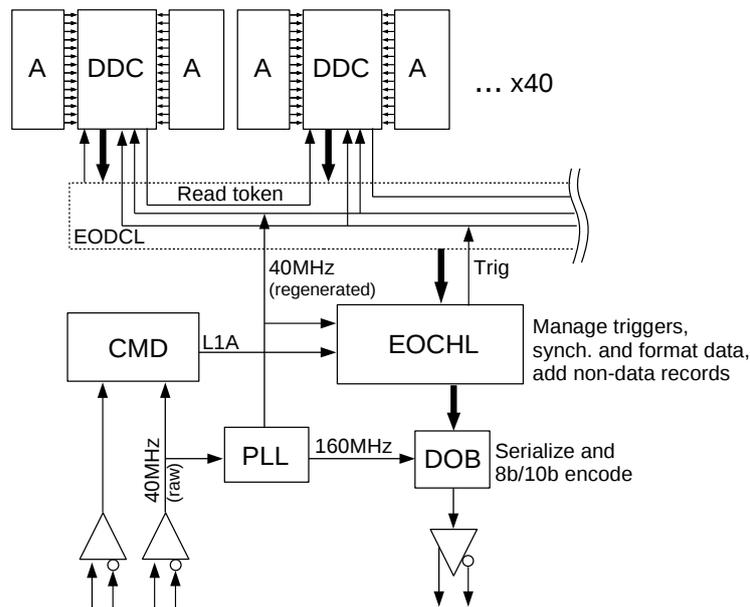
### 4.3 Analog Array and Biases



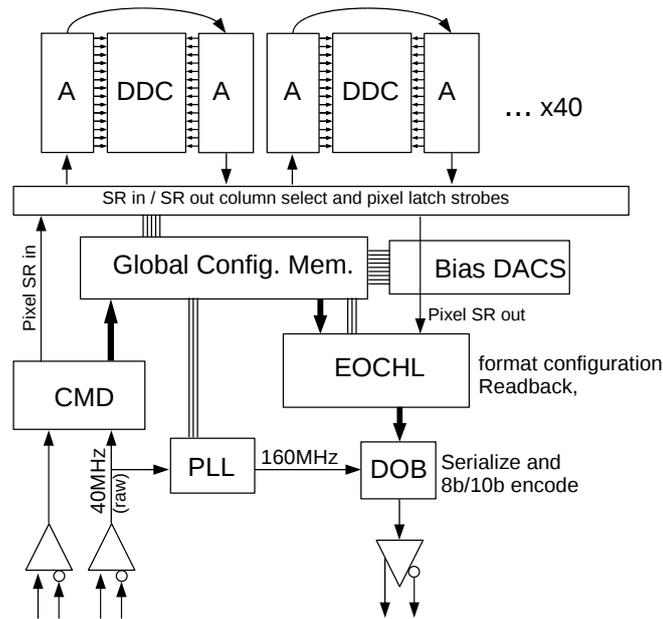
**Figure 5:** FE-I4 chip diagram, not to scale. The coordinate origin is at the bottom left corner, with  $x$  increasing to the right and  $y$  increasing upwards.



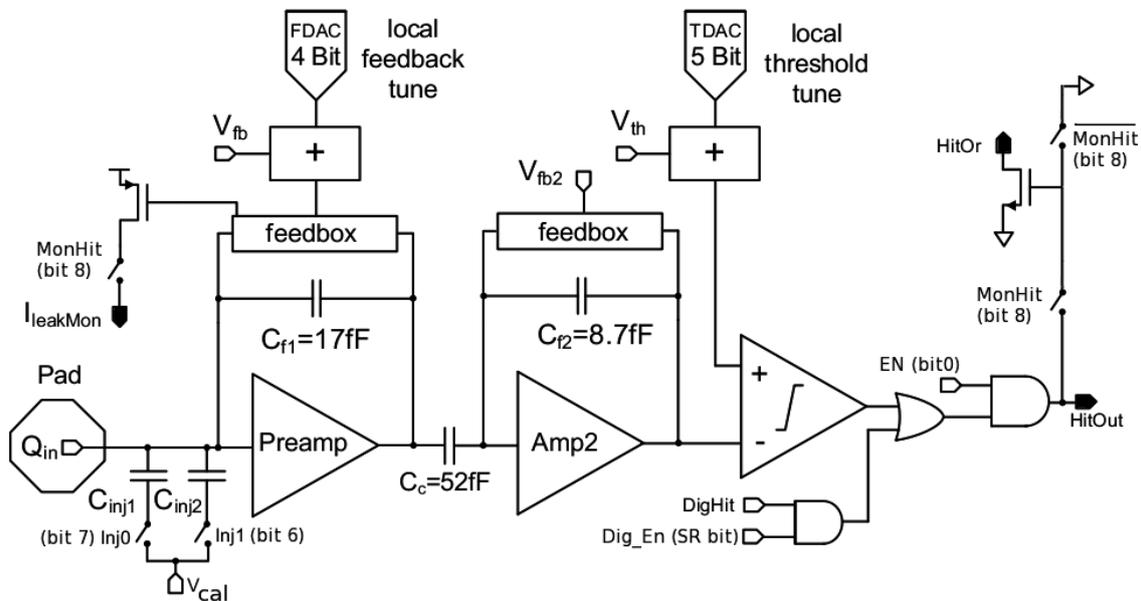
**Figure 6:** Simulated data losses for FE-I4 and FE-I3 chips placed at 3.7 cm from proton-proton beam collisions at 14 TeV. The expected number of interactions per beam crossings during IBL operation is 75.



**Figure 7:** Simplified schematic of the output data path in a typical data acquisition configuration. Circuit blocks shown are analog column (A), digital double column (DDC), end of digital column logic (EODCL), command decoder (CMD), phase locked loop clock multiplier (PLL), end of chip logic (EOCHL), and data output block (DOB).



**Figure 8:** Simplified schematic of the configuration path for typical single-chip operation. Circuit blocks shown are analog column (A), digital double column (DDC), global configuration memory, analog bias digital to analog converters (DACs), command decoder (CMD), phase locked loop clock multiplier (PLL), end of chip logic (EOCHL), and data output block (DOB).



**Figure 9:** Analog pixel schematic diagram. Output pins are solid, input pins are open.

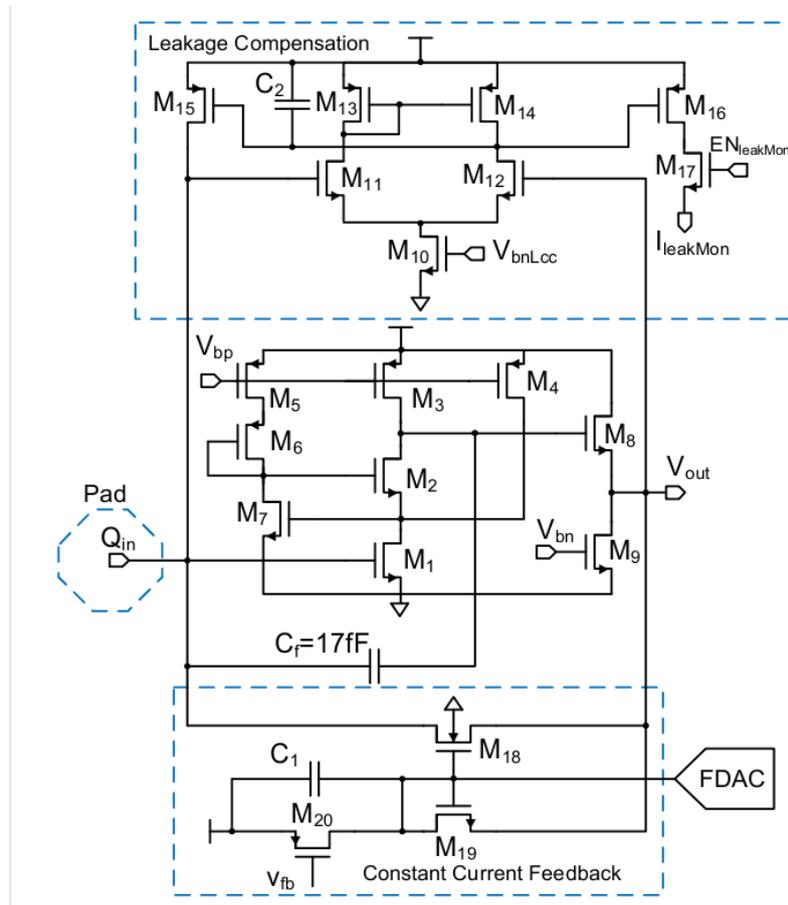


Figure 10: Analog front end preamp circuit schematic.

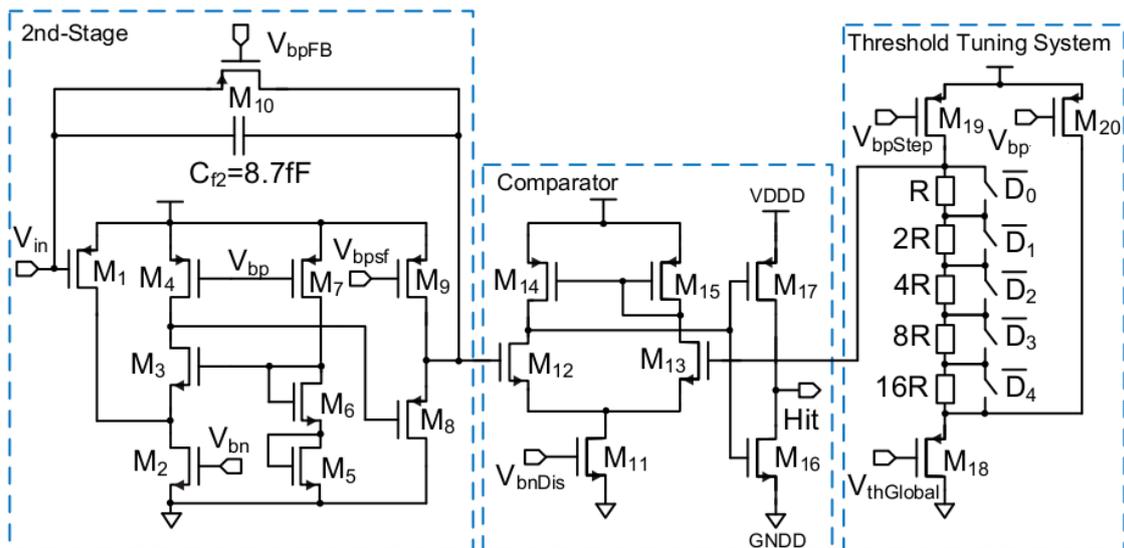
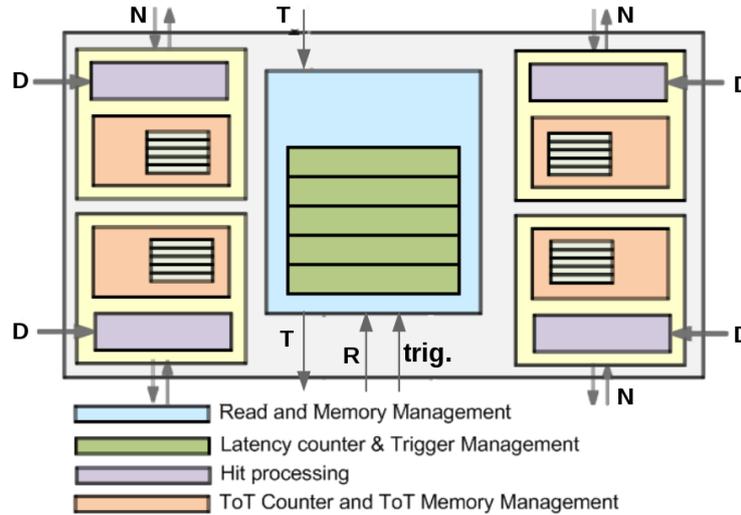


Figure 11: Second stage and discriminator circuit schematic.

#### 4.4 DDC, PDR, and EODCL

The FE-I4 contains 40 Digital Double Columns (DDC) connected together via the End of Double Column Logic (EODCL). Each DDC contains 168 Pixel Digital Regions (PDR) grouped into 7 units of 24 PDRs each. Each PDR processes the data from 4 pixel discriminators (2 rows by 2 columns). The PDR is designed and synthesized as a single logic block: it cannot be subdivided into 4 “pixel” blocks (see Figure 12). The PDR contains 5 latency calculation and triggering units



**Figure 12:** Diagram of the Pixel Digital Region circuit. The selected connections shown are: trigger input, analog discriminator inputs (D), neighbor logic inputs and outputs (N), read token in and out (T), and read signal input (R).

that are PDR-specific, not pixel specific. The time stamping of a hit is hence common information to the region. However, pulse-height information (ToT) is independently counted for each pixel. The PDR contains 4 groups of 5 pixel memories, where each memory stores 4 bits of ToT plus a 1 bit neighbor flag. The digital threshold is applied to the discriminator output of each pixel prior to starting a dedicated 4-bit binary counter for ToT. This is done with a shift register adjustable between 1 and 3 cells (1 cell for digital threshold 0 to 3 for digital threshold 2). If the input and output of the shift register are both high, then the hit has passed the digital threshold and is considered a “big hit”. The reset value of the ToT counter is 1111, and for pixels whose analog discriminator did not fire, this is the value that will remain as the ToT code meaning “no hit”. Whenever the analog discriminator does fire, the counter is decremented to 1110, which means “small hit”, but does not automatically continue to count until the digital threshold shift register has finished shifting. If the digital threshold is passed (big hit), the counter is cleared to 0000 and starts to count. Otherwise it remains at the 1110 code for small hit. The counter stops either when the analog discriminator falls or when it reaches 1101. The resulting ToT counter values vs. actual analog discriminator pulse width and digital threshold setting are listed in Table 7.

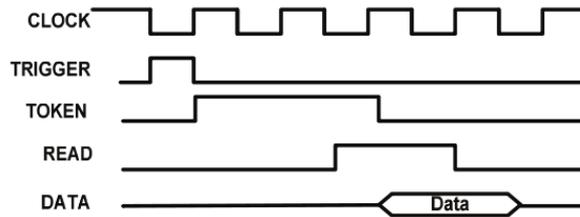
Whenever the digital threshold is passed by any of the 4 pixels (indicating the presence of a

"True" ToT (clocks)	HitDiscCnfg			
	00	01	10	11
Below tresh	F	F	F	x
1	0	E	E	x
2	1	0	E	x
3	2	1	0	x
4	3	2	1	x
5	4	3	2	x
6	5	4	3	x
7	6	5	4	x
8	7	6	5	x
9	8	7	6	x
10	9	8	7	x
11	A	9	8	x
12	B	A	9	x
13	C	B	A	x
14	D	C	B	x
15	D	D	C	x
≥16	D	D	D	x

**Table 7:** ToT 4-bit code values (hex) for actual time over threshold values (left column) and hit discrimination configuration settings. Setting "11" is not valid and will result in hit output being completely disabled. The values above the dividing line in the central 3 columns will only be read out if they are next to a "big hit" – all values below the line are "big hits".

big hit), the next available latency counter is started and a busy flag is set for that counter. The next available counter is calculated by combinatorial logic from the busy flags of the 5 counters, in order to avoid having a register based pointer that could be vulnerable to SEU. Each latency counter is mapped one to one with four ToT memories, one per pixel, avoiding the need for a pointer mechanism which would be vulnerable to SEU. One clock after a latency counter starts, the PDR will be ready to start another counter, should another big hit occur. Thus the fact that timing is common to the whole region does not result in any dead time penalty. The "pile-up" dead time (a new hit arriving while a given discriminator is still high from a previous one) affects only single analog pixels and not the whole PDR as if it were one big pixel. Furthermore, a new big hit in the PDR does not truncate or otherwise affect the ToT values of the previous hits, even if there are ToT counters still counting when the new big hit arrives. ToT counters are always allowed to finish counting and their values stored in the ToT memory associated to the time of arrival of the hit. This does not add any dead time, because the 4 ToT counters are independent. Any dead-time is already present at the analog discriminator: there is no advantage to not counting ToT as long as the analog discriminator is high. Of course, for a hit to be possible there must be at least one analog discriminator that is low and therefore at least one ToT counter that is idle. While the "big hit status" of each pixel is allowed to persist for only one clock cycle, a "small hit status" persists

690 for 2 clock cycles. Thus the ToT code for small hit will be recorded if it was present either at the same time as a big hit or in the clock after. Each pixel has one neighbor: above (below) in the same column for the pixels at the top (bottom) of the PDR. If the neighbor's status shows a small hit during at the time a big hit occurs or in the clock after, the neighbor bit is latched, if it shows a big hit or no hit then it is not latched.



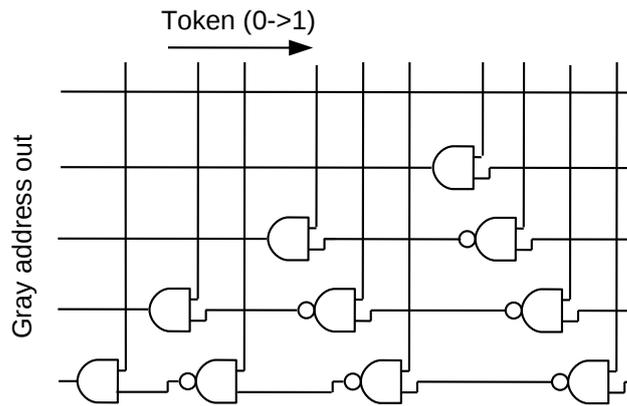
**Figure 13:** Example of PDR readout timing.

695 While the DDC contains 168 PDRs it also contains additional elements for signal distribution and is thus a single circuit with inputs from 336 discriminators plus 336 enable signals, half from each left and right sides. The readout of hit data is on two common buses (data and address) and is prioritized by a token organized as a chain of OR gates, triplicated for redundancy with majority voting in every region. The token moves from the DDC top (row 1) to the bottom (row  
700 336). A readout signal causes the PDR with the token to output its data and advance the token (Figure 13). The output data bus consists of 25 bits (16 ToT + 4 neighbor bits + 5 Hamming error protection codes) implemented also with daisy-chained OR gates to avoid the need to drive large wire loads. The 11 bit address bus (8 address + 4 protection bits) is organized as a thermal Gray encoder (Figure 14). This minimizes the number of gates used to generate and transmit the address.  
705 Minimum number of gates in turn minimizes area and power, and maximizes yield. A Gray code address bus for N regions needs only N gates for the entire bus. Hamming code protection increases the number to just over 3N. The readout operation is controlled by the read signal in each PDR that holds the token and enables the data transfer of the requested triggered event. Any region with the read signal set holds the token temporarily while placing its data on the bus. Otherwise the token  
710 passes though each region in a time given by one OR gate delay.

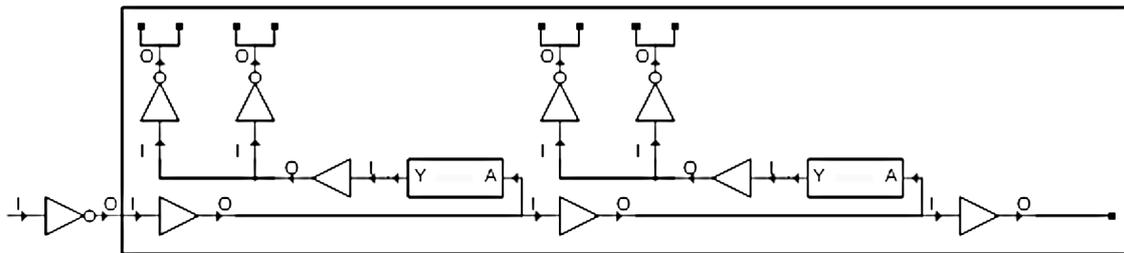
Need to explain how the trigger ID, trigger ID request and latency comparison are done.

Every PDR needs the 40 MHz system clock. A simple regeneration scenario with balancing is used to distribute the clock with small skew (Figure 15). Some level of mismatch is purposely left uncorrected to preserve a clock skew of about 2 ns, since a perfectly unskewed clock distribution  
715 may lead to very sharp power spikes. The trigger signal is distributed in the same way. All other global signals needed by the PDR do not have critical timing and therefore use a simpler distribution scheme as shown in Figure 16.

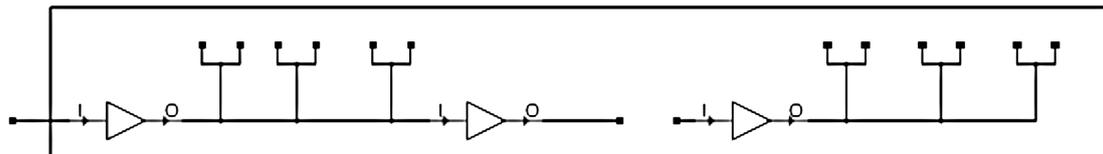
The DDC power distribution is done with full custom layout in the low resistance top metal layers. This achieves a calculated DDC voltage drop of 10 mV assuming 40 mA per PDR average  
720 current consumption (this is the total digital current budget for the chip divided by the number of PDRs). The DDC circuitry is designed entirely using high level description and synthesized with standard cell libraries. However, Each PDR is placed over its own substrate isolation implant, as are all remaining DDC buffers and delays. Finally, each PDR contains a full custom decoupling



**Figure 14:** Example of Gray address thermal encoder. The encoder inputs are along the top and are initially all 0. As the token advances from left to right each successive input switches from 0 to 1. This causes the encoder output to present 00000, 00001, 00011, 00010, 00110, etc., where the rightmost bit is at the bottom of the figure. There is one gate per input.



**Figure 15:** Simplified schematic of clock and trigger distribution in the DDC. The rectangles are delay elements.

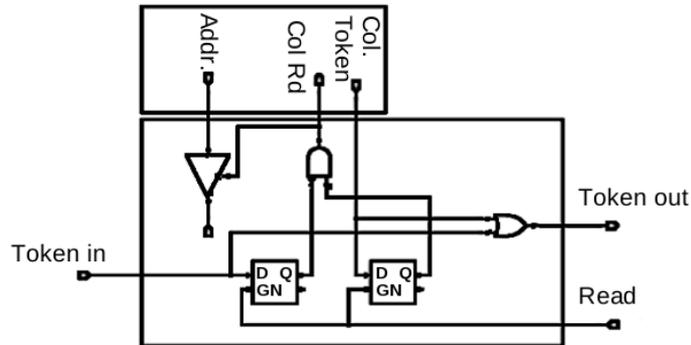


**Figure 16:** Simplified schematic of distribution non-critical timing signals in the DDC.

capacitance of ?? pF. The actual PDR power consumption after physical implementation was simulated to be 6.6  $\mu$ W/pixel (average) in the typical process corner at 25°C and 1.2 V, with hit rate  
 725 corresponding to 75 interactions per beam crossing at 3.7 cm radius, and 100 kHz trigger rate with latency of 120 crossings.

The EODCL distributes the read token, control signals, and data among the 40 DDCs. There is only one read token for the entire array. All 40 columns are controlled in parallel and read out  
 730 sequentially. Despite the large size of the FE-I4, parallel readout was not needed to meet the trigger rate specifications. The EODCL contains simple logic to select each column for readout as shown

in Figure 17. A token similar to the DDC token runs along the EODCL and generates the column address based on its position.



**Figure 17:** Simplified schematic end of column signal routing in EODCL

#### 4.5 End of Chip Logic

735 The End Of Chip Logic is responsible for several tasks:

- Receive data from the columns,
- Unpack data, arrange into pixel pairs and re-pack for output,
- Temporarily store output data in a asynchronous Fifo,
- Generate the Bunch Counter value (BCID),
- 740 • Generate the Trigger Id,
- Generate multiple triggers,
- Merge service records into the data stream,
- Merge configuration read back records in the data stream,
- Receive bits from the pixel shift register, pack them and merge into the data stream.

745 All logic for these tasks is triplicated with majority voting at the output, to make it SEU safe. All data in this block are stored in Hamming Code for the same reason. All counters are triple redundant, with the value of each bit updated from the majority output on every clock.

A schematic of the EOCHL is shown in Figure 18. It is made up of the following circuit blocks, each one represented by a box in the figure: Read Out Controller, Error Handler, Reset Deglitcher, Data Formatter, and Shift Register. The Read Out Controller generates all the signals needed to read data from the pixel array using a state machine, receives all data, and prepares it for output to the data output block. Hit data are received from the EODCL and fed through the Data  
750 Formatter to first unpack them into single pixel values and then combine two pixels into one data

record as efficiently as possible. This is called dynamic phi pairing, explained by the following  
 755 algorithm: (1) take all hits in the same column, including neighbor hits; (2) list them in ascending  
 row; (3) use the first hit column and row address for the first data record, and place the ToT value  
 in the first ToT field; (4) if the next hit has a row number greater by exactly 1, then place its ToT  
 code in the second ToT field and advance to the following hit; (5) otherwise place the “no hit”  
 code in second ToT field and process the next hit as a new record; (6) repeat until there are no  
 760 more hits in the column. The Data Formatter also adds a header in front of the data, containing the  
 BCID, the trigger ID, and a flag to indicate if any service records are ready to be read out. The data  
 format including headers and all record types is described in detail in Section 9. The Error Handler  
 receives error pulses from the rest of the chip, counts them in 32 separate categories (given in the  
 Appendix), and produces service records to report errors off chip. The Shift Register is not actually  
 765 a shift register, but rather the block that processes the output of the column shift registers and packs  
 it into address and value records. The data from global configuration registers for read-back is also  
 received by this circuit.

#### 4.5.1 Readout Controller

Figure 19 shows a schematic of the Readout Controller. Data records are received from the Data  
 770 Formatter, Shift Register, or Error Handler via the Data Concentrator. Each record is then Hamming  
 coded and written into the FIFO via the Data Switch. The FIFO is 8 bits deep by 36 bits wide,  
 including the Hamming code bits. The FIFO is written with the same system clock as used by the  
 pixel array, but it is read out with the FIFO Read signal generated by the DOB. This allows using an  
 asynchronous clock for data output. The output of the FIFO is Hamming decoded before sending  
 775 to the DOB.

The data flow through the FIFO proceeds via the Input multiplexer to select data source, the  
 Hamming Encoding, the Data switch, the FIFO proper, and finally the Hamming Decoder. The  
 Input multiplexer has 3 data sources: hit data via the Data Formatter, Configuration Register Data  
 (both value and address), and Service Records from the Error Handler. Additionally, the FIFO has  
 780 a 4<sup>th</sup> input source which is the Bunch Counter and contains the data header fixed bits. The data  
 flow through this block is combinatorial. The header bits are already Hamming Coded, while the  
 Hamming code for all other data is calculated prior to writing into the FIFO.

The Data Switch has two inputs and one output. The inputs are Hamming encoded data or  
 Header. The output is controlled by a register needed to avoid timing errors: when the fifo is full  
 785 the register is frozen until the “full” signal is removed. The FIFO provides buffering between Data  
 Formatter and the DOB. The write and read sides of the FIFO work in their own clock domain with  
 double clock synchronization blocks for the addresses in between. This synchronization generates  
 the Fifo\_Full and Fifo\_Empty signals. The Hamming decoder converts the 36-bit wide FIFO con-  
 tents to the 3-byte wide (24 bits) data stream. The decoders can correct up to one error in each 8-bit  
 790 output data word. Additionally, if an error is detected an error signal is sent to the Error Handler.

The Readout Controller has the following counters: trigger multiplication counter, level-1  
 trigger ID counter (L1\_Trig\_Id), bunch crossing counter (BC), L1 trigger input to EODCL counter  
 (L1In), trigger request to EODCL counter (L1Req), and skipped trigger counter. Each counter is  
 triplicated with majority voting logic on the output. Every clock cycle a new value is loaded into  
 795 the counter from the output of the majority vote, so a SEU will be automatically corrected. Two

registers are used to keep track of triggers sent to the EODCL and pending for readout: the L1 register and the BC register. The L1 register is 16 bits (each triple redundant) and keeps track of the 16 possible trigger slots. For each trigger pulse sent to the EODCL the corresponding bit in the L1 register is set. The position of the bit for each trigger pulse is given by the L1In counter value. When event data for a given trigger have been read out, the corresponding bit is cleared. The position of the bit for the event being read out is given by the L1Req counter value. The BC register contains 16 Hamming coded words. Each word contains an 8-bit (plus Hamming code) bunch crossing ID (given by the BC counter value) and a 7-bit (plus Hamming code) level-1 trigger ID (given by the L1\_Trig\_Id counter value). There is a one to one correspondence between L1 counter bits and BC counter words. The values stored in the BC register are sent out as part of the Data Header. An “event” is labeled by these values.

When L1 trigger command is received by the chip, the Trigger Generator produces a burst of trigger pulses given by the the value programmed in the Trig\_Cnt global register (see Appendix C). This is done by presetting a the 4-bit trigger multiplication counter to the Trig\_Cnt value and, when a trigger command arrives, counting down to zero. During this time trigger pulses are sent to the EODCL (one per clock) and counted by the L1In counter. Each trigger pulse is half a period long and high during the low phase of the clock. All pulses in the burst are marked with the same Trigger ID in the BC register, which is the value of the L1\_Trig\_Id counter. This is a 7-bit counter incremented when trigger commands are received by the chip. The bunch crossing ID, on the other hand, is different or each pulse, given by the BC counter. This is an 8-bit counter of the 40 MHz clock. The BC counter is zeroed by the RD2bar reset and also by the bunch counter reset command.

The L1In is a 4 bit counter which serves as a write pointer for the L1 and BC registers, and its value is also sent to the EODCL to be used as an internal trigger identifier in the pixel array. The L1In counter is incremented for every L1 pulse sent to the EODCL. Note this is more frequently than every L1 trigger command sent to the chip when the trigger multiplier is set different to a value other than 1 (the value 0 results in 16 pulses). The L1Req is a separate 4-bit counter which serves as a read pointer for the L1 and BC registers, and is also sent to the EODCL in order to select all the data from this specific trigger. This counter is increased by the Readout State machine after an event is finished reading out. Both the L1In and L1Req values are only used internally and not copied to the output data stream.

The skipped counter counts trigger pulses not sent to the columns because the L1 register is full. These triggers are ignored. The counter is 8 bits. The read out of the counter is done by the command decoder. Reading the counter also clears its content.

#### 4.5.2 Readout Processor

The Readout Processor is the state machine that organizes the readout cycle activities. Figure 20 shows a flow chart of the state machine. This orders the processing of hit data, configuration data, and service records. The first test point in the state machine checks if the data acquisition is enabled and if there has been a trigger for the given L1Req number. When both conditions are met a readout cycle will start. Once a readout cycle starts the event is always finished completely before any other action. Note that in FE-I4A there is no event timeout and it is possible for all pixels to have a hit at the same time, in which case the readout cycle will last a long time. The Read Out cycle has the following steps:

1. Wait 3 clocks for the token to arrive from the EODCL.
2. If Token is through, send Read pulse to the EODCL.
- 840 3. Wait 3 clocks for hit data and new token.
4. Place data in the Data Formatter and check token for more data.
5. If more data, repeat the steps 3 and 4 until token is false.
6. Check if a service word has to be sent (see below).
7. Go back to the starting point.

845 In case of no hit data the state machine will check if Configuration Address and Value words are pending. The Configuration Address is optional and can be disabled by a configuration register bit. When the Data Acquisition is disabled, multiple Configuration Address and Value words can be sent out in one block. This must be the case in order to process data from the column shift registers. A Service Request command always sends out 32 service words and a null word. A  
 850 single Service Record will also be sent automatically at the end of each hit data event hit data, in case Service Records are pending. Note that even if error pulses have been received by the Error Handler, Service Records will not come out automatically unless there are triggers given to the chip which result in hit data output.

### 4.5.3 Error Handler

855 Logging of error signals is accomplished by 32 identical Error loggers in the Error Handler block. Each Error logger has a synchronous rising edge detector followed by a 10-bit counter. When a rising edge is detected, the Error output is set, and the counter is incremented. The counter stops at the maximum value of all 1's. The counter is reset during the read cycle. All 32 Error output signals are connected to an Error Control module. If any Error logger has detected an error, the  
 860 module Error Control will send a Write\_Service\_Record signal to the Readout Controller. In the data stream, a service record will be added after the data header and a flag is set in the Data Header. The service record contains 16 bits of payload, consisting of the address of the Error logger and the value of the counter. This automatic service record generation can be masked off with the Error Mask register. Sending a ReadErrorReq signal will output 32 service records (regardless of the  
 865 error mask bits) and will reset all the error counters (this signal is generated with the Global Pulse command).

## 4.6 Data Output Block



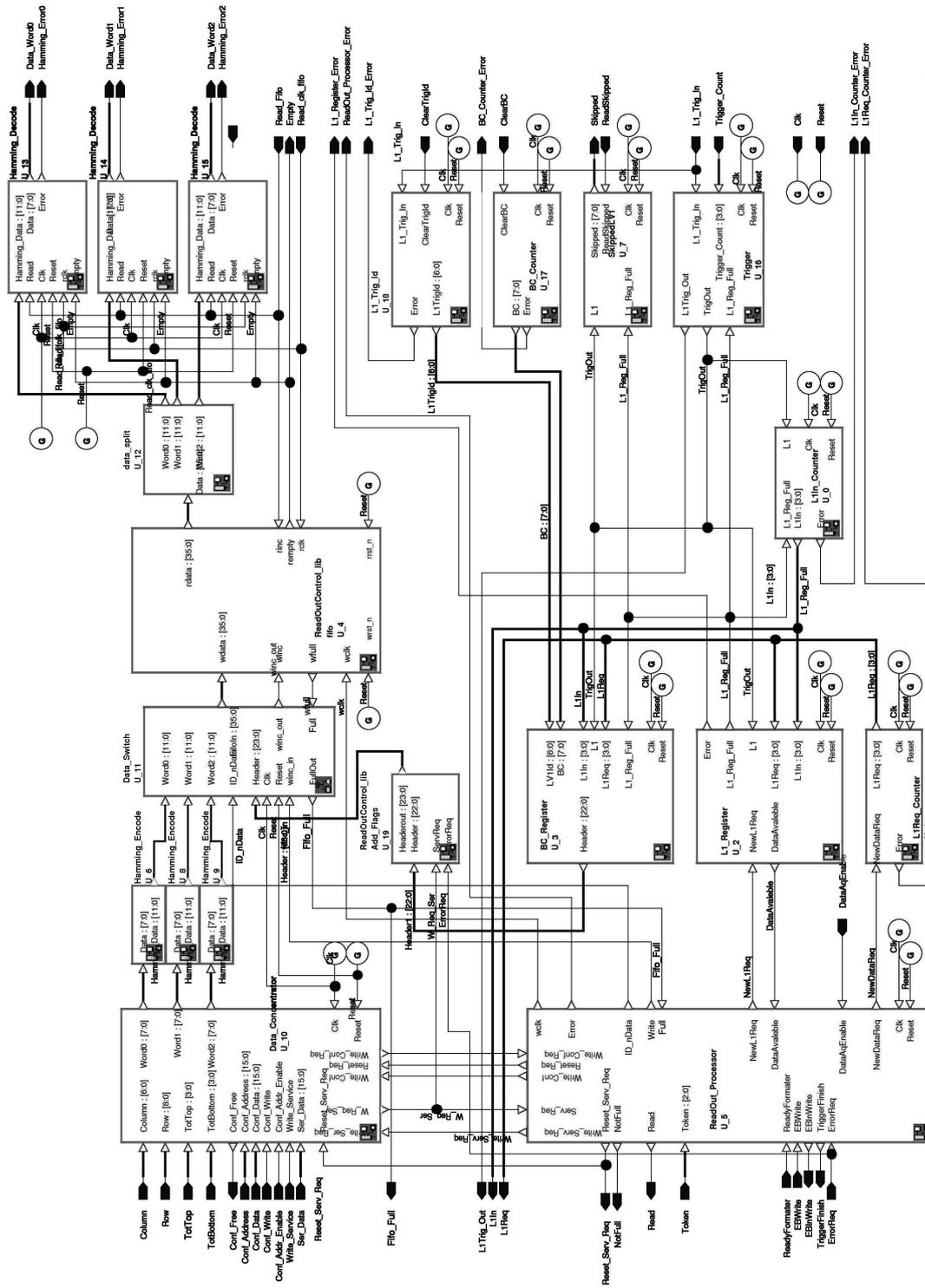


Figure 19: High level schematic of the End Of Chip Logic block

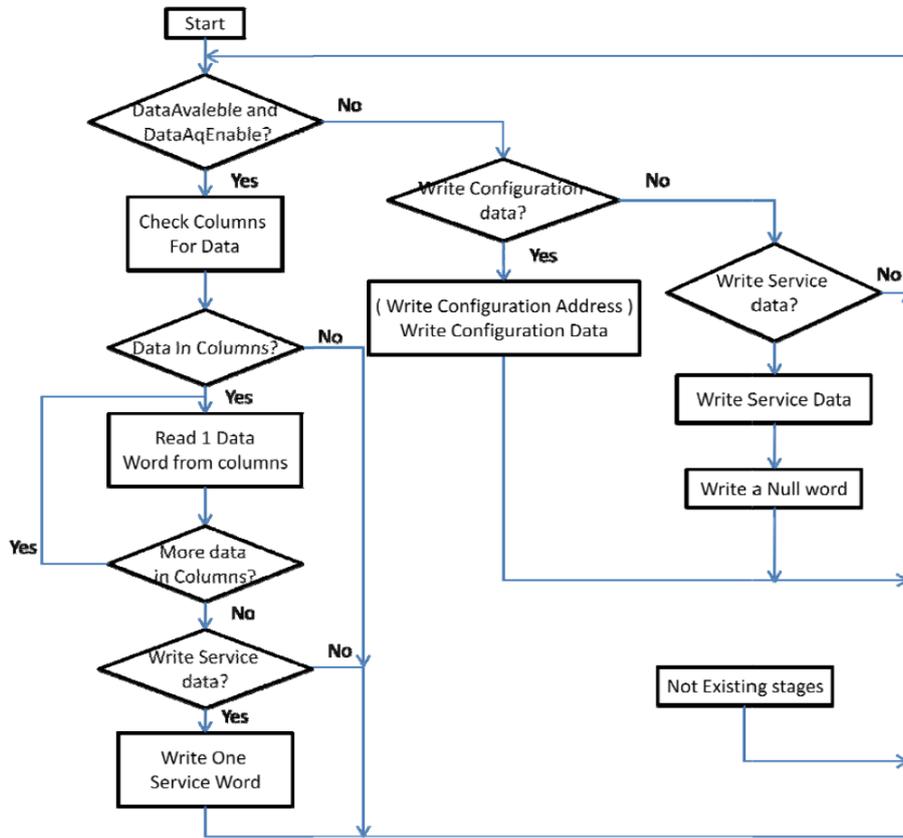


Figure 20: Flow chart of Readout Processor state machine.

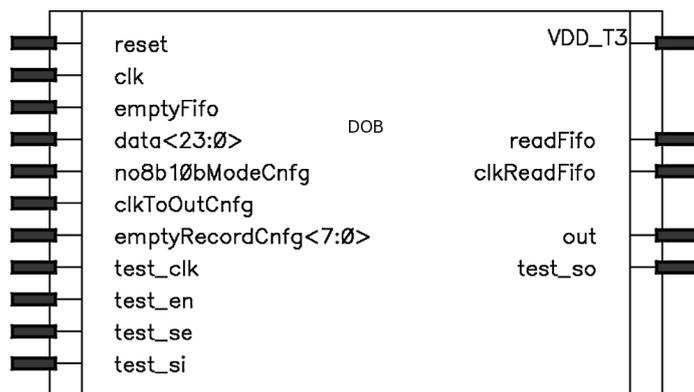


Figure 21: Data Output Block Symbol

## 4.7 Clock Generator

The clock generator block contains two parts: a Phase Locked Loop (PLL) core that generates  
 870 different clock frequencies, and a multiplexer (MUX) output stage that selects what signal to send  
 to each of two outputs going to the rest of the FE-I4 chip. The PLL core has a dedicated power pin at  
 the chip level, as well as an enable signal in the chip global configuration— both must be present for  
 operation. Figure 22 shows the circuit schematic. The PLL is a classical (type II) architecture with  
 a Phase Frequency Detector (PFD), a Charge Pump (CP), a Loop Filter (LF), a Voltage Controlled  
 875 Oscillator (VCO) and Dividers (DIVs). The nominal oscillating frequency of the VCO in the PLL  
 is  $f_{VCO} = 640$  MHz. The multiplication factor of the PLL is  $N = f_{VCO}/f_{REF} = 16$ .

Internally dividing down a high frequency naturally leads to output clocks with a 50% duty  
 cycle even for an unbalanced reference clock. In addition, a higher output frequency of the VCO  
 results in smaller capacitance values in the LF. The capacitances of the LF take up about one third  
 880 of the area of the PLL core. The capacitors are of vertical natural capacitors (VNCAP) type from  
 metal layers 1 to 3. The LP consists of three capacitors with capacitance values of 319 fF, 710 fF  
 and 7.43 pF plus one additional 710 fF capacitor that decouples the supply voltages. The block  
 uses standard library cells for all digital logic, placed in a common T3 deep implant for substrate  
 isolation. The custom circuits (PFD, CP, and LF) use triple well transistors for regular  $V_t$  and RF  
 885 types.

The CLKGEN signals are single-ended CMOS (nominal 1.2 V). The nominal input reference  
 clock is  $f_{REF} = 40$  MHz. The PLL generates  $\times 8$ ,  $\times 4$ ,  $\times 2$ , and  $\times 1$  clocks waveforms with 50%  
 duty, with a constant phase relationship to the input reference (the exact phase difference will be  
 process and temperature dependent). Each multiplication ratio has an independent enable so that  
 890 switching noise can be minimized by disabling buffers for unwanted ratios. The  $\times 16$   $f_{VCO}$  is used  
 to synchronize all lower frequency outputs, and so is slightly ahead in phase. The two CLKGEN  
 outputs (CLK0\_OUT and CLK1\_OUT) can each provide any of the internally generated clocks  
 (40M\_se, 80M\_se, 160M\_se, 320M\_se, but not the 640 MHz clock signal), the input reference  
 clock (RefCLK) or an auxiliary clock (AuxCLK) that is an external input for the CLKGEN block.  
 895 The output selection is controlled by a global configuration register (6 bits total, 3 for each output).  
 The independent power makes it possible to completely disable the PLL and still operate the MUX  
 to provide either RefCLK or AuxCLK to the rest of the chip.

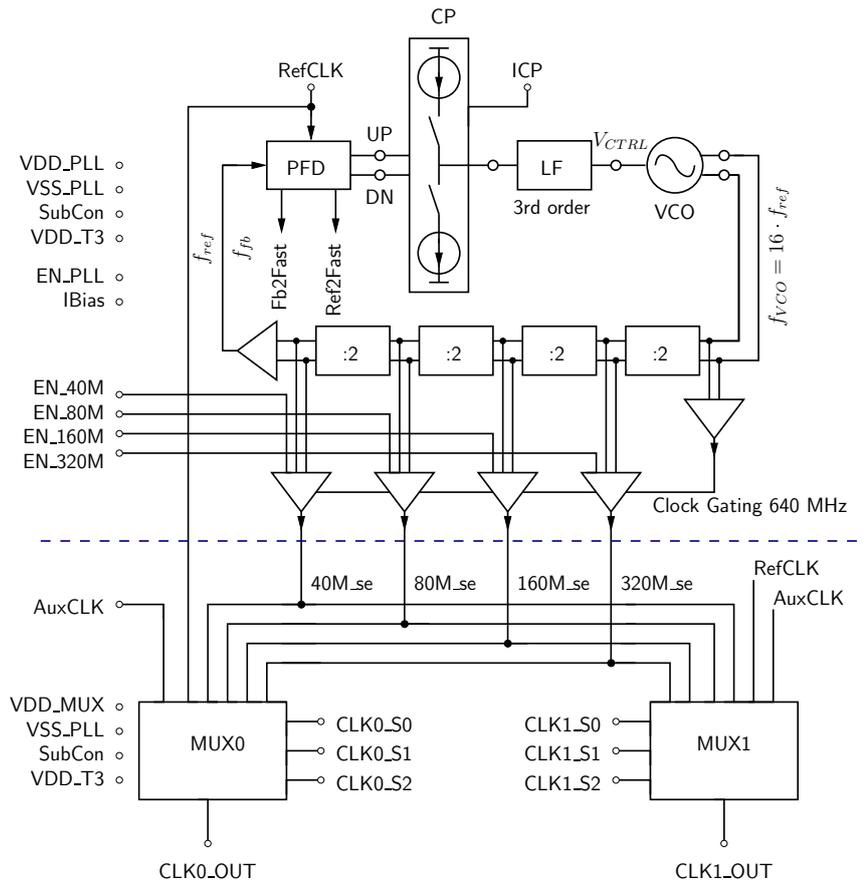
CLK0\_OUT feeds the data output block and thus controls the output data rate, while CLK1\_OUT  
 feeds the end of chip logic and the digital array, which nominally run at 40 MHz. The  $\times 1$  ratio is  
 900 desirable for CLK1\_OUT, because it will have 50% cycle and low jitter even if the reference clock  
 is of poor quality. Note that the generated clocks are multiples of the input reference clock, thus,  
 for example, the name 80M\_se really means  $f_{REF} \times 2$  and not exactly 80 MHz.

Two outputs (Fb2Fast and Ref2Fast) provide error flags if the PLL does not acquire a stable  
 lock on the input reference clock. Internally the CP of the PLL is controlled by a signal called  
 905 UP and a signal called DN. When the PLL has acquired a lock, both UP and DN signal lines will  
 stay high only for a very small fraction of the time of the reference clock period. If one of the  
 signals is high for a longer time, that indicates that the control loop senses a need to adjust the  
 VCO oscillation frequency. This corresponds to a loss of lock. If the VCO oscillates too fast with  
 respect to the multiplied reference clock ( $N \cdot f_{REF}$ ), the signal Fb2Fast will be high. If the VCO

910 oscillates too slow with respect to the multiplied reference clock, the signal Ref2Fast will be high. During start-up, one or both will be high until lock is established- typically less than  $5 \mu s$ . These lines are monitored within the chip and rising edges counted as errors and reported (see Section ??). If Fb2Fast or Ref2Fast are permanently high this might indicate that the PLL is out of locking range (see Table 8), which may be due to the reference clock input or the PLL supply voltage level  
 915 - a higher supply voltage will result in faster oscillation of the VCO.

The performance specifications of the CLKGEN block, based on simulations and on measurements done on a demonstrator chip are listed in Table 8. The two bias currents shown in the table are provided by the BIASDACS block and programmed with global configuration registers. They can also be overridden by providing the bias current directly to the corresponding pads. Both  
 920 currents flow into NMOS current sinks. The CLK0\_OUT output of the CLKGEN block can be directly monitored on the chip LVDS output by putting the DOB block into clock loop back mode, and one can make use of this feature for standalone operation. The required contacts and settings for operating the CLKGEN block as a standalone circuit are summarized in Table 9.

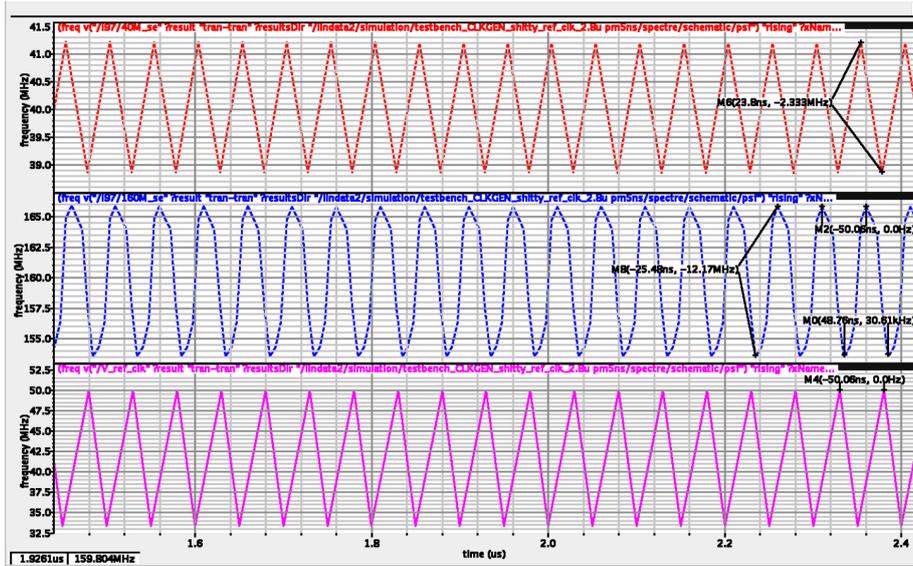
The measurements on a demonstrator chip are limited by available instruments to input reference clock jitter RMS of 2 ps and output frequency of 160 MHz. However, since the lower frequency  
 925 clocks are internally generated from the higher frequency clocks, the encouraging results



**Figure 22:** Clock Generator Schematic

indicate proper functioning of the (unobserved) higher frequency clocks. These measurements also include the performance characteristics of the LVDS drivers integrated into the output pads of the demonstrator. The results are summarized in Table 10.

930 The CLKGEN single event transient (SET) cross-section is unknown as it could not be simulated. The cross-section will strongly depend on the layout. None of the CLKGEN sub-blocks has been designed with special SET-hardened architecture. However, in case of a loss of lock due to SET, the PLL core will reacquire lock in the same way as it does during normal settling. SET recovery was simulated by charge injections of 3 pC in 1.5 ns at various nodes of the PLL core circuit. In all cases lock was reacquired in times of order 1  $\mu$ s.



**Figure 23:** CLKGEN output frequency (top:  $\times 1$ , middle:  $\times 4$ ) for bottom input reference clock having a variation of  $\pm 5$  ns

In the IBL application of FE-I4 the 40 MHz input reference clock will be delivered from a

Specification	Unit	min	nom	max
Supply Voltage ( $V_{DD\_PLL}$ , $V_{DD\_MUX}$ )	V	N/A	1.2	1.5
Clock Multiplier $N$	-	-	16	-
General Bias $I_{BIAS}$	$\mu$ A	60	80	250
Charge Pump Reference current $I_{CP}$	$\mu$ A	N/A	10	N/A
Input Reference Clock Frequency $f_{REF}$	MHz	21	40	61
VCO Oscillation Frequency $f_{OSC}$	MHz	336	640	976
Peak Current Consumption $I_{PEAK}$	mA	4.6	5.3	5.7
Average Current Consumption $I_{DC}$	mA	2.7	3.4	3.7
Settling Time (2% accuracy) $t_{SETTLE}$	$\mu$ s	0.9	0.9	1.1

**Table 8:** Performance Specifications for the CLKGEN Block

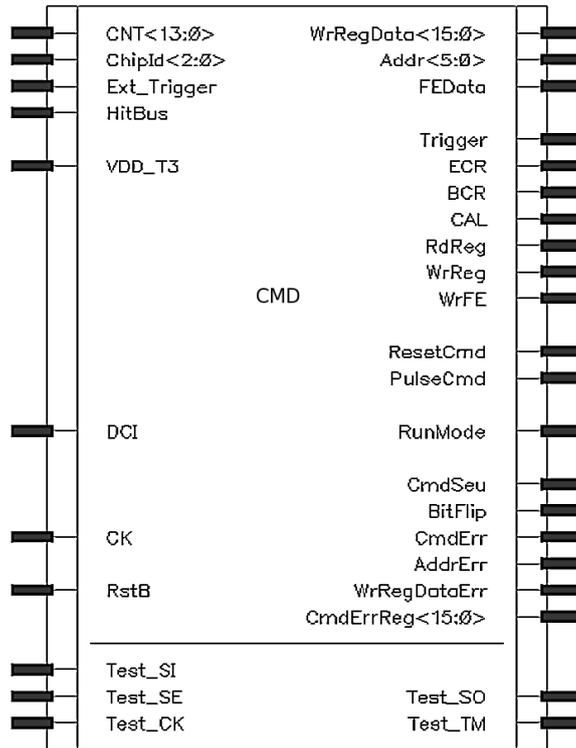
custom optical to electrical converter called DORIC. The DORIC generated clock behaves like a superposition of two 20 MHz clock signal that do not have a fixed alignment in time but rather vary by  $\pm 5$  ns upon start-up and by  $\pm 0.5$  ns after parameter tuning. The  $\pm 5$  ns ( $\pm 0.5$  ns) variation of the period length between two consecutive edges corresponds to a input reference clock of the PLL varying between 33 MHz (39.2 MHz) and 50 MHz (40.8 MHz) in contrast to the ideal 40 MHz. Simulation results for the worst case are depicted in Figure 23. It can be seen that the PLL smooths out the frequency variation of the input reference clock by about a factor of 7.

#### 4.8 Command Decoder

The command decoder (CMD) is responsible for interpreting the serial commands to control the chip. All valid commands can be found in Section 6.3. The CMD circuit is completely synchronous using the input clock provided externally with no option to use a different clock. The serial input is sampled on the rising edge of the clock and each sample is interpreted as a bit. The input bit stream is continuously parsed searching for valid command patterns. Patterns not corresponding to a command sequence are ignored. Once a command is found the full number of bits expected for that command are recorded before searching for a new command. The processing is done by a state machine. The CMD control generates internal logic signals that control the various blocks of the chip. All internal signals going to other blocks are synchronized with the rising edge of the clock. The CMD symbol is shown in Figure 24.

Internal net	Wire bond Pad(s)	Configuration register
VDD_PLL	VDD_PLL	–
VDD_T3	VDDT3_Shield	–
VDD_MUX	VDDD2	–
VSS_PLL	GND_PLL	–
SubCon	VSS	–
IBias	PIIbias_P	PIIbias or SRAB 24-31
ICP	PIIcp_P	PIIcp or SRAB 32-39
EN_PLL	–	EN_PLL
EN_320M, EN_160M	–	EN_320M, EN_160M or SRAB 80-81
EN_80M, EN_40M	–	EN_80M, EN_40M or SRAB 88-89
CLK0_S2 - CLK0_S0	–	CLK0 or SRAB 82-84
–	–	clk2OutCnfg
RefCLK	Ref_Clk_N	–
	Ref_Clk_P	–
CLK0_OUT	DOB_OUT_N	lvdsDrvEN
	DOB_OUT_P	lvdsDrvEN

**Table 9:** Summary of required connections and settings for standalone operation of the clock generator block. Internal nets refer to the schematic. See the appendix for the specific number of each wire bond pad or configuration register.



**Figure 24:** Command Decoder Symbol

955 The CMD state machine is triplicated, so that there are actually three distinct copies inside the FE-14 and all CMD outputs are selected with a majority voting circuit. Each copy processes the input serial stream independently and in parallel. Because each state machine returns to its idle state after a finite amount of time (usually after a small number of clock cycles), there is a very small probability that bit-flips in any state machine will cause the majority voting circuit to be incorrect.

960 Errors can happen only if SEU bit-flips occur in two different state machine status registers within the time it takes either one to return to the idle state. Even in such a case, as soon as the first of the two affected state machines returns to its idle state, the majority voting output would again be correct. In addition to the majority voting circuit there is an XOR tree of all triplicated outputs

	Reference in	CLKGEN out				
Frequency [MHz]	40	40	80	160	320	640
Jitter pk-pk [ps]	44	82	74	94	70	106
$\sigma$ -Frequency [kHz]	6.5	19	79	258	1710	8100
$\sigma$ -Period [ps]	4.1	12	12	11	17	20
Duty Cycle Deviation [%]	–	0.24	0.33	0.1	n.m. <sup>1</sup>	n.m.

1: n.m. stands for not measured

**Table 10:** Measurements of CLKGEN Signal Integrity

in order to calculate, once every clock cycle, if there has been a detection of a SEU anywhere  
 965 inside the Command Decoder. Whenever this happens a 5-bit counter is incremented and its non-  
 overrunning value is stored inside the CMD in register CmdErrReg[15:10]. Additionally, a pulse  
 on the CmdSeu internal net is sent to the End of Chip Logic (EOCHL), which will independently  
 count the errors and produce a service record.

The command communication protocol is designed to allow single bit flips on the input se-  
 970 rial stream without generating errors. If such a BitFlip is detected when there are no commands  
 recognized, a non-overrunning, internal counter is incremented and its value is stored in CmdEr-  
 rReg[9:5]. If the BitFlip occurs during a Trigger command the Command Decoder will detect it  
 and increment a 3-bit, non-overrunning counter stored in CmdErrReg[4:2], but still decode the cor-  
 responding trigger correctly. In addition to that there is the ability to detect a BitFlip during the  
 975 Fast or Slow header. The occurrence of these events is flagged (but not counted) in the CmdEr-  
 rReg[1:0]. In addition to that the logical OR of these three errors (Trigger, Fast header, Slow  
 header) will generate a CmdErr error signal sent to the EOCHL.

Internally, the CMD controls the 6-bit global register address bus and the 16-bit register write  
 value. The Address and the WrRegister storage inside the CMD are also triplicated or SEU pro-  
 980 tected. This triplication includes error correction whenever triple redundant mismatch is detected.  
 If an error is detected the AddrErr and WrRegDataErr signals are generated and sent to the EOCHL  
 in order to allow the counting of these types of errors.

The whole CMD can be reset using the external RD1bar, negative logic signal. However, since  
 the CMD is completely synchronous, the clock must be running in order for to reset to operate. No  
 985 serial command exists for resetting the CMD state machine. The global reset command produces  
 BCR and ECR signals that are sent to the EOCHL and also causes a reset of the internal CMD error  
 counters described earlier. The ECR command does not clear the CMD error counters.

To allow quality assurance testing that is sensitive even to failures that would be masked by  
 the triple redundant design, a Scan Chain has been implemented. There are four dedicated Scan  
 990 Ports that can be accessed via the IOMUX block.

- Test\_SE: Scan Enable port. Scan circuitry is active when it is high.
- Test\_CK: Scan test clock.
- Test\_SI: Input of the scan chain circuitry.
- Test\_SO: Output of the scan chain circuitry.

995 All flip-flops in the CMD circuit are included in the scan chain when in test mode. There  
 are 246 D flip-flops and 224 of them are implemented as multiplexed scan flip-flops, while the  
 remaining 22 are already connected as shift registers inside the design.

## 4.9 Global Configuration Memory (CNFGMEM)

### 4.10 EFUSE

1000 The EFUSE block consists of a bank of triple redundant RAM of the same design as the CNFGMEM,  
 but with an additional parallel write bus connect to a bank of non-volatile ROM based on E-  
 fuses. There are 4 16-bit words for a total of 48 bits. The arrangement is shown schematically

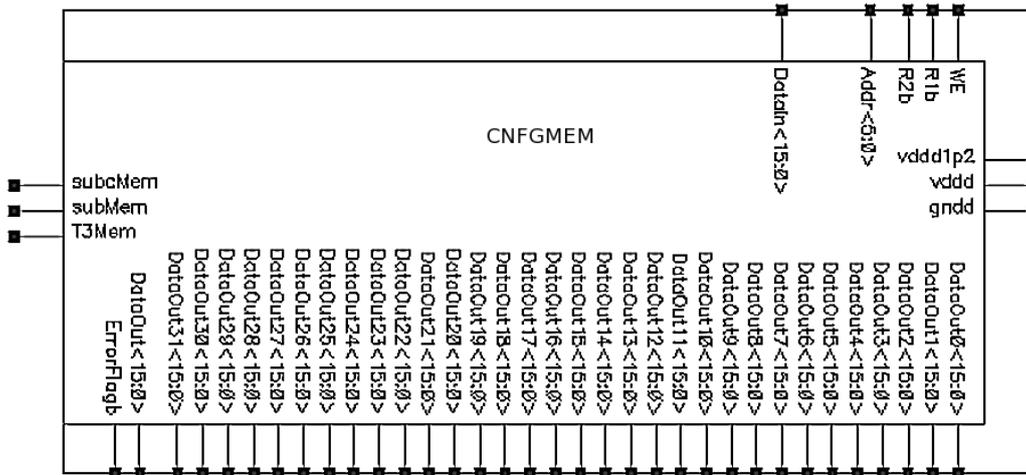


Figure 25: Configuration Memory Symbol

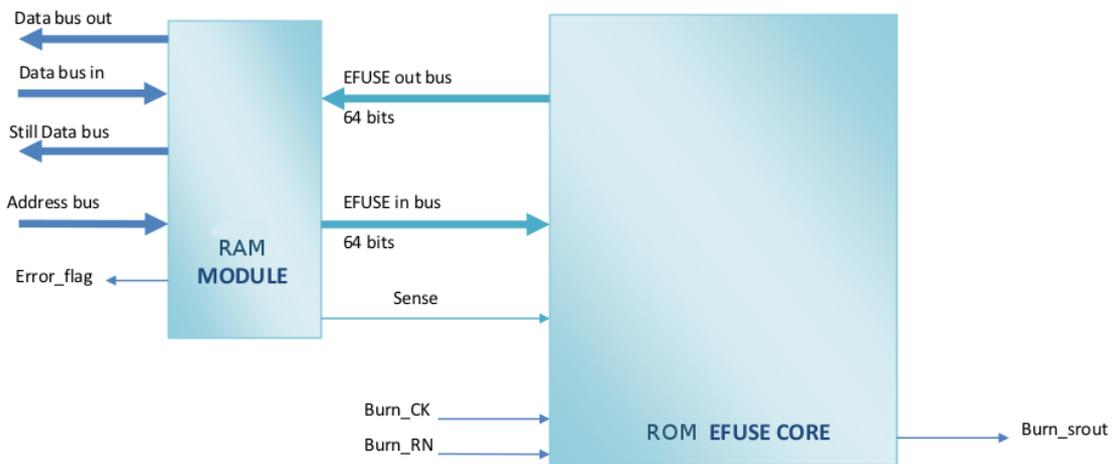
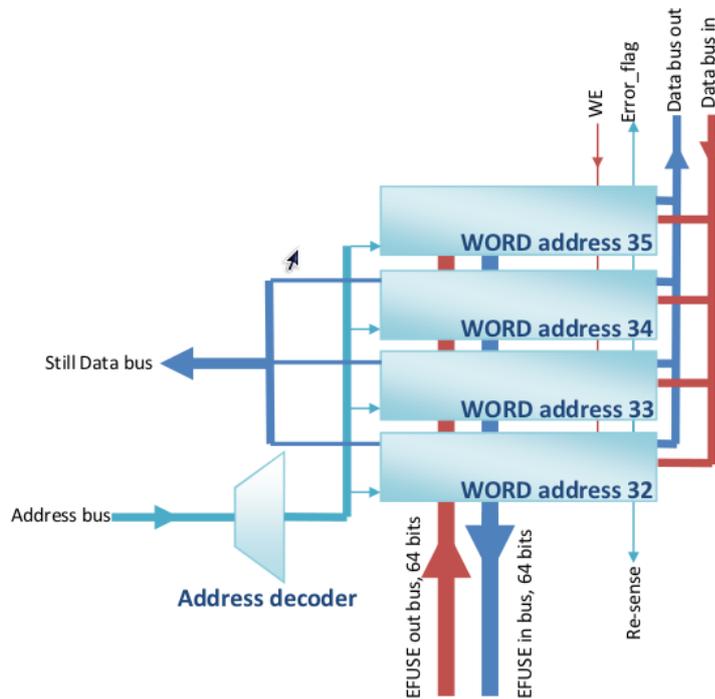


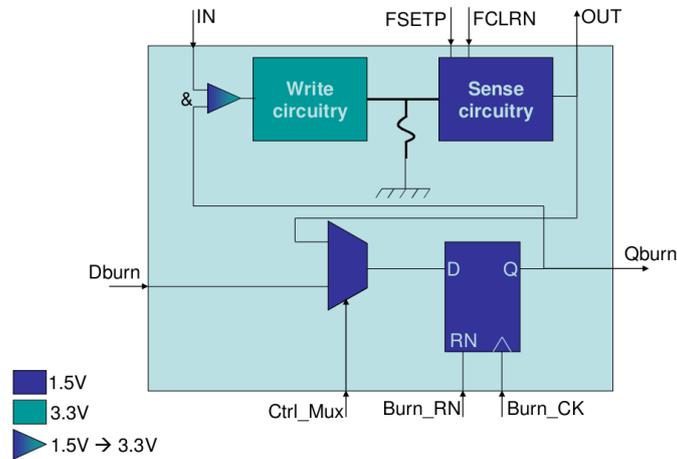
Figure 26: Block diagram of the EFUSE circuit

in Fig. 26. An E-fuse is a special resistor that has a value between 50 and 150  $\Omega$  as fabricated, but which can be reliably altered to permanently increase its resistance above 5 k $\Omega$  by applying 3.3 V across it for approximately 1 ms. The programming current during burn-in will be of the order of 10 mA. The resistance can be sensed by applying a brief (< 100 ns) 100 mV pulse, without any damage. The E-fuse can survive millions of sense cycles, but not much higher numbers. The resistance cannot be continuously sampled, nor can it be sampled at a high frequency without racing an excessive number of read cycles. For these reasons the EFUSE block, as far as the rest of the chip knows, is just 4 more words of RAM the same as the CNFGMEM, with the added feature that this RAM can be loaded from E-fuse ROM instead of with a write register command. This is also convenient to program the E-fuse ROM, which can be done by first writing the EFUSE RAM just like normal configuration registers, and then burning the written values into the E-fuses. Alternatively, one can choose to not make use of the E-fuses at all, and just use the EFUSE block



**Figure 27:** RAM block of the EFUSE

1015 as additional configuration RAM.

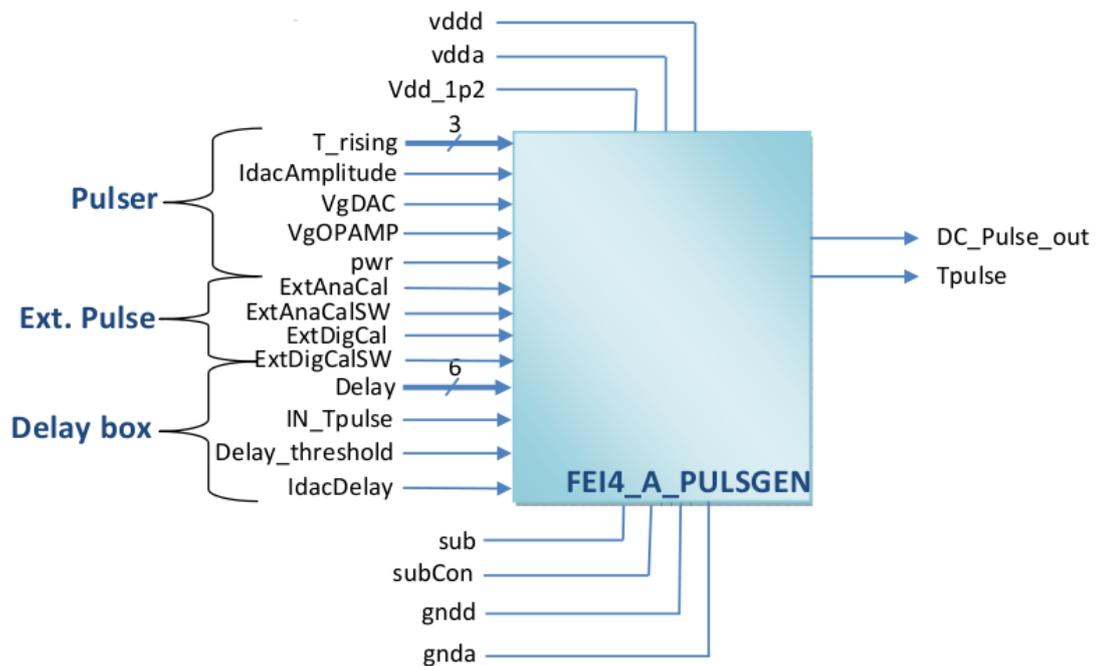


**Figure 28:** RAM block of the EFUSE

1020 Burning the E-fuses cannot be done for all 48 bits in parallel, because this would draw 500 mA of current. Instead the E-fuses are selected for burn-in one-at-a-time by employing a shift register loaded with a single one followed by 47 zeros. The EFUSE reset signal prepares the shift register this way. The shift register must then be advanced by an externally supplied CMOS clock (this clock is supplied via the IOMUX block). A single cell of the ROM core block is shown in Fig. 28. This

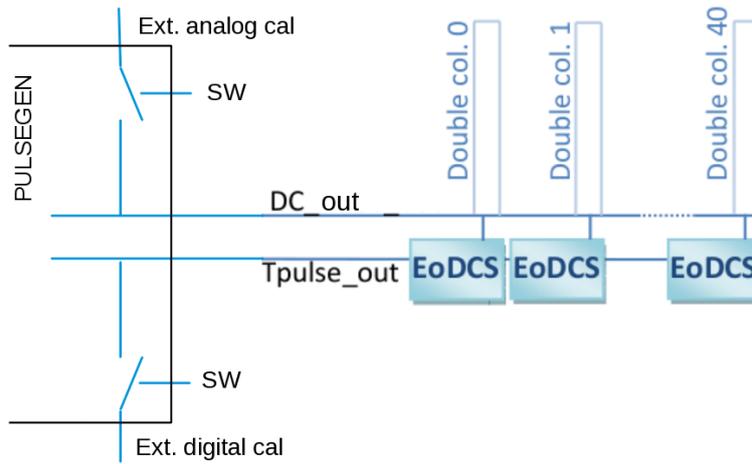
shows schematically the E-fuse resistor, together with a write block, a read block, and one state of the control shift register. This shift register can also be used to read the E-fuse values through the IOMUX block, rather than loading them into the EFUSE RAM. This could be useful to retrieve the serial number of broken chips that cannot be operated normally, but where the EUSE block by itself may still be powered, or for debugging purposes. The FSTEP and FCLR signals are internally generated by a built-in sequencer with a timing specified by the chip foundry. Also the sense circuit design is provided by the foundry.

#### 4.11 Pulse Generator



**Figure 29:** Block diagram of the PULSEGEN block.

The PULSGEN block can be thought of as a pulse generator instrument, with a digital and an analog output that can be routed to the pixel array. The input capacitance of the full array has been estimated from 40 pF to 80 pF. The analog pulse fall time must be faster than 10 ns to avoid any ballistic deficit (charge injection happens on the falling edge) and the rise time must be hundreds of microseconds to avoid any baseline due to reverse charge injection. The PULSEGEN has a programmable delay line with range of 50 ns and 1 ns or better resolution. In practice the PULSEGEN generates a DC voltage and a gate signal (with programmable delay) that controls 41 end-of-double-column choppers in parallel. This results in a fast fall time. The slow rising back to quiescent DC is ensured by a very weak PMOS transistor in triode mode. The rise time is adjusted by varying the size of the PMOS transistor (implemented as an array). The programmable delay is generated by a voltage ramp and a comparator. The discriminator threshold is fixed and the ramp rate is adjustable. The ramp uses a current supply from the bias generator and can be disabled by setting this current to zero. Varying the ramp current results in the delay changing non-linearly (as



**Figure 30:** Distribution of the PULSEGEN signals to the columns.

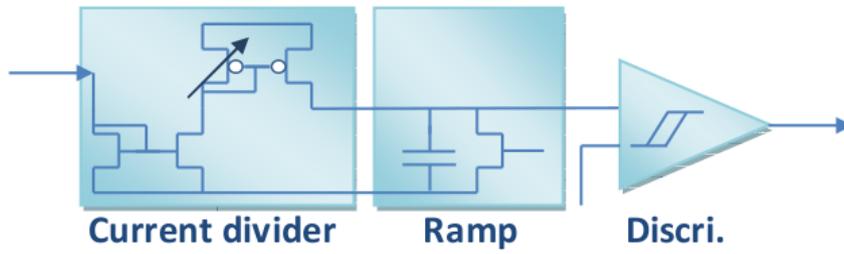
the inverse of current). Instead, the current can be fixed and a divider in the ramp generator can be varied, resulting in a linear delay change with divider setting. Setting the divider to its maximum value disables it. The entire pulse generator can also be bypassed, allowing external injection. For external injection a digital pulse and DC voltage, or an external analog pulse, have to be supplied. A block diagram of the PULSEGEN block is shown in Fig. 29. The distribution of signals to columns is illustrated in Fig. 30. Note that the same digital pulse output can be used for digital injection or to control the chopper circuits for analog injection. While the delay is adjustable, the width of the digital pulse is simple equal to the width of the pulse used to trigger the PULSEGEN, which can be produced by the CMD CAL command or by a global pulse command (either CMD or external).

A diagram of the delay generator is shown in Fig. 31. It shows the current divider, ramp generator and discriminator. The threshold voltage is tied to the voltage reference, which is internally set to  $VDDA/2$  in FE-I4A. The current divider uses a NMOS mirror followed by a programmable, unbalanced PMOS mirror to divide the input current depending of the value programmed. The output current is given by eq. 4.1,

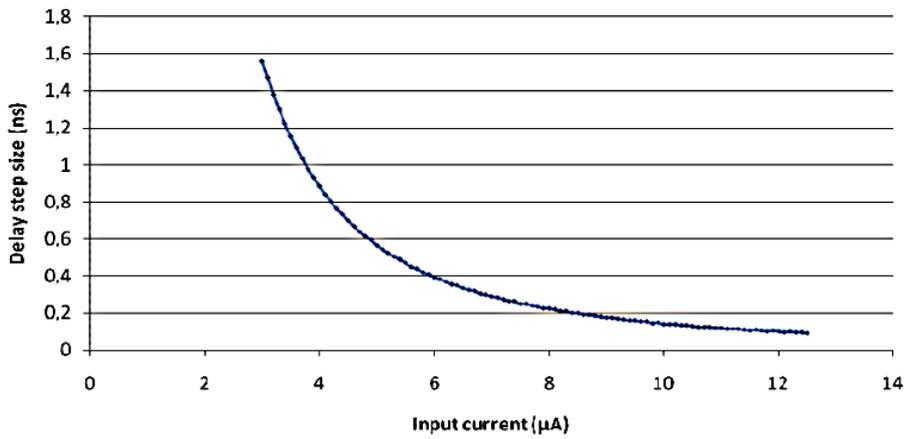
$$I_{out} = \left(1 + \frac{1}{10N}\right)I_{in} \quad (4.1)$$

where  $N$  is the input code (6 bit),  $I_{in}$  is the input current supplied by the bias generator block, and  $I_{out}$  is the output current. Setting  $N$  to its maximum value will actually bypass the divider entirely, making  $I_{out} \equiv I_{in}$ .

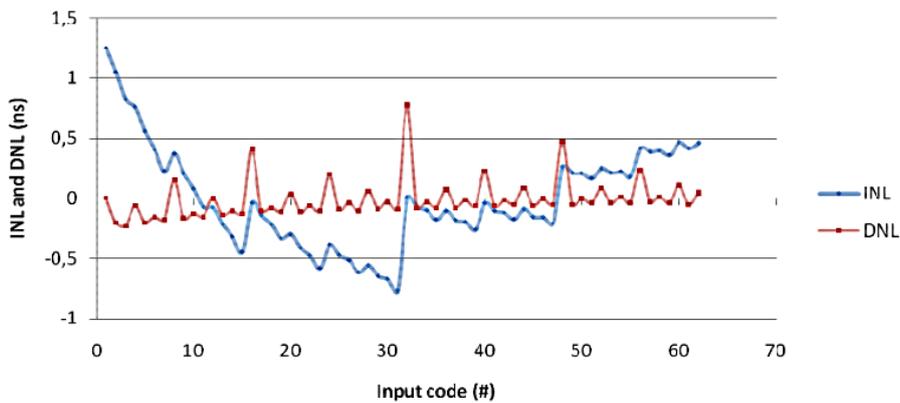
The ramp generator is a simple capacitance  $C$  with a charge-compensated injection switch. When the  $T_{pulse}$  signal is low, the capacitance is shorted by the switch and the output ramp signal is tied to ground. When  $T_{pulse}$  goes high, the input current charges the capacitance giving a ramp slope  $I_{out}/C$ . When the current divider is used to set the delay, the input current  $I_{in}$  defines the step size, and the delay is simply equal the the divider setting times the step size (with small nonlinearities shown below), plus a constant offset predicted to be 18 ns. The simulated value of step size vs. input current is shown in Fig. 32, while the differential and integral nonlinearity simulation predictions are shown in Fig. 33. When the divider is bypassed (by programming the maximum value), the simulated delay vs. input current is shown in Fig. 34.



**Figure 31:** Diagram of the delay generator in the PULSEGEN block.

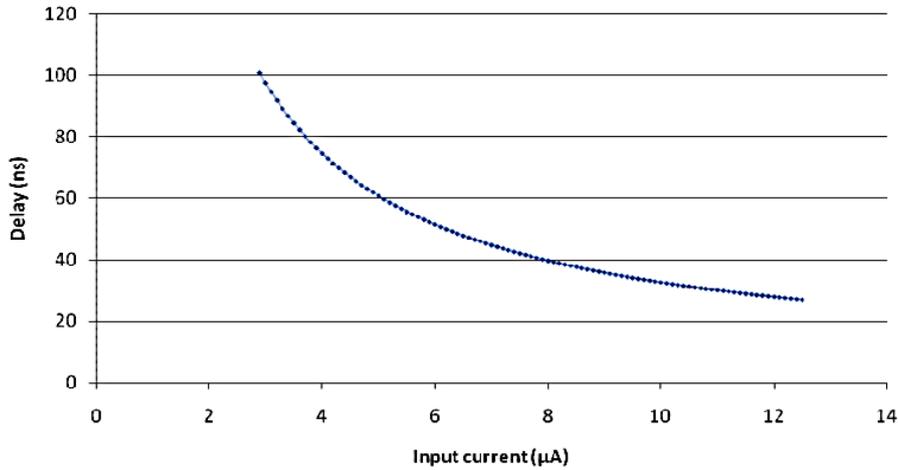


**Figure 32:** Simulated delay step size vs. input current.



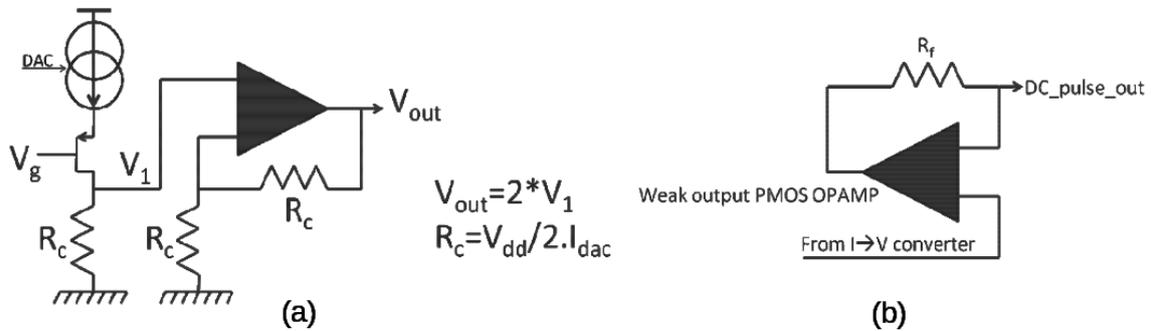
**Figure 33:** Simulated differential and integral nonlinearities of the delay generator when using the current divider.

The DC voltage output is generated in two stages: a current to voltage converter to transform an input current to a rail to rail output voltage, followed by a sense circuit to correct the voltage for an expected offset due to the leakage current of the pixel matrix. The sense circuit also serves as a high impedance output leading to the required long rise time of the injection pulse at the pixel inputs.



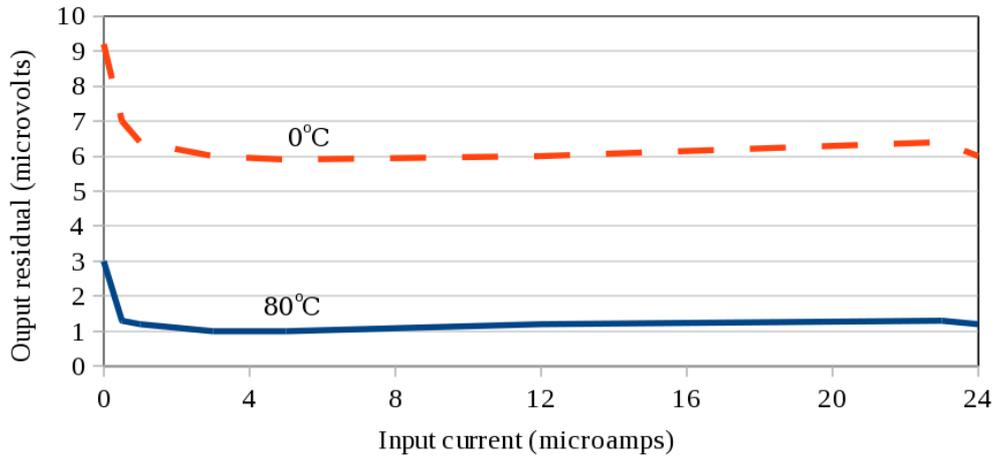
**Figure 34:** Simulated delay as a function of input current when the current divider is bypassed.

The input current is provided by a 10-bit DAC in the bias generator (not part of the PULSEGEN block). The current to voltage converter is based on the generic FEIA\_A\_OPAMP block, described separately. The circuit is a resistor, chosen to produce 750 mV at maximum current, followed by a non-inverting gain 2 amplifier, to achieve rail-to-rail output (Fig. 35(a)). The cascade transistor is there to present a constant voltage to the output of the DAC supplying the current. The deviation of the output from a linear ( $V=I_{in} \cdot VDD/I_{max}$ ) at different temperatures, from simulation, is shown in Fig. 36.

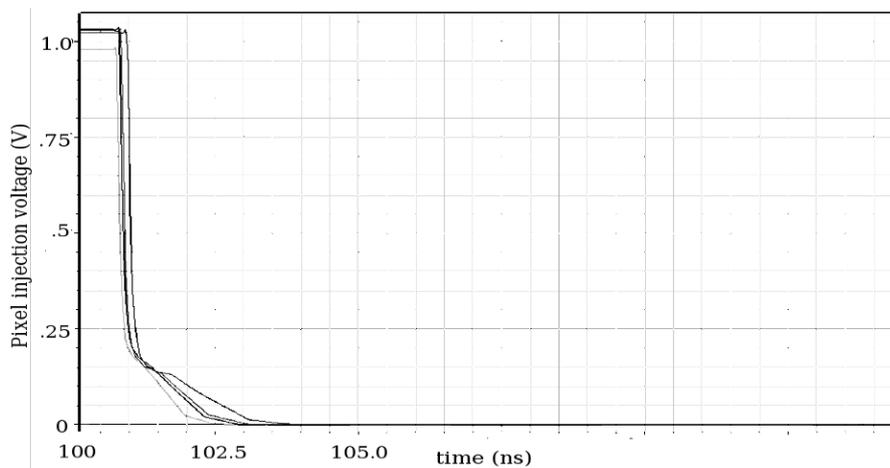


**Figure 35:** Schematic of (a) the current to voltage converter, and (b) the output sense circuit.

The output voltage must have high impedance to produce a long rise time to DC quiescent after each falling edge. This high impedance leads to an offset due to leakage current in the large matrix of pixels. A passive high impedance output would have an offset of over 100 mV due to pixel leakage. Therefore, an active feedback system senses the leakage current and compensates for the offset. The compensation uses a modified version of the FEI4\_A\_OPAMP with a weak output connected as shown in Fig 35(b). A row of 8 switchable PMOS is used to allow 3-bit control rising edge slope. A 100 k feedback resistor increases the output impedance. The rise time from 0 to 1 V varies from 25 µs for 000 setting to 750 µs for 111. A simulation of the fall time when driving the



**Figure 36:** Simulated output voltage residual of current to voltage converter.



**Figure 37:** Simulated fall time in 4 process corners, when driving the full pixel array. An arbitrary delay value is shown, with the PULSEGEN triggered at  $t=0$ .

full array, as seen by one arbitrary pixel, is shown in Fig. 37. Four process corners are overlaid in the same plot.

#### 4.12 Shunt-LDO Regulators

1090 The Shunt-LDO regulator is a combination of a low-drop linear voltage regulator and a shunt regulator. The Shunt-LDO regulator can be configured as a pure linear voltage regulator for usage in a conventional voltage based supply scheme. In addition, the regulator provides dedicated shunt circuitry which can be enabled for application in a current based serially powered supply scheme. There are two Shunt-LDO regulators in FE-I4B, one on the far left (back row of bond pads, intended to supply analog voltage) and the other on the far right (intended to supply digital voltage).  
1095

A simplified circuit of the Shunt-LDO regulator is shown in Fig. 38 and the inputs and outputs are listed in Table 11. The LDO regulator part is formed by the error amplifier A1, the PMOS



transistor M1 given by the aspect ratio  $k$  of the current mirror formed by transistor M1 and M2, is  
 1110 drained into the gate-drain connected transistor M5. The amplifier A2 and the cascode transistor  
 M3 are added to improve the mirroring accuracy. The reference current which depends on the input  
 potential REG\_IN is drained into the gate-drain connected transistor M6. The reference current is  
 compared to the fraction of current flowing through transistor M1 by use of the differential amplifier  
 A3. If the current drained to transistor M6 is smaller than the reference current, the shunt transistor  
 1115 M4 is steered to draw more current and vice versa. By this means, a constant current independent  
 of the regulator load is flowing through transistor M1 with a value defined by:

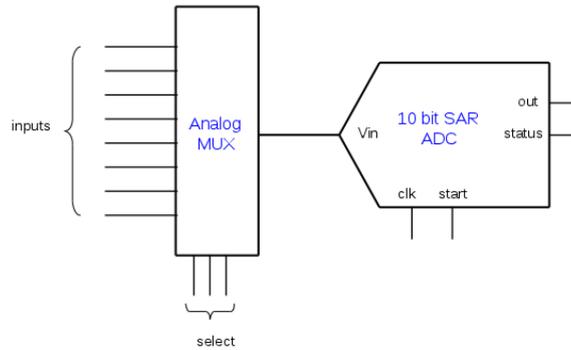
$$I_{in} \approx k \frac{V_{in} - V_{thM6}}{R3} \quad (4.2)$$

where  $V_{thM6}$  is the threshold voltage of transistor M6. The resistor R3 is integrated internally and  
 has a resistance of 8 k $\Omega$  (16 k $\Omega$ ) for the analog (digital) regulator of FE-I4B. These values have  
 been chosen to reduce current draw fluctuations in the IBL implementation, but are too large (too  
 1120 little current) for a serial power application. Resistor R3 is used for the reference current definition  
 if the VDDShunt port is connected externally to REG\_IN. However the reference current can be  
 increased to any desired value by adding an external resistor in parallel to R3, between Rext and  
 REG\_IN (note that VDDShunt must still be powered for the shunt circuitry to work). Alternately,  
 a resistor from Rext to REG\_GND will "steal" current from R3 and will therefore reduce the shunt  
 1125 current (a short to REG\_GND will zero the shunt current). With 2 k $\Omega$  resistance (parallel sum of  
 external resistor plus R3), a maximum shunt current of 500 mA can be reached. Shunt operation is  
 disabled by shorting the Rext and VDDShunt ports to the local ground port REG\_OUT.

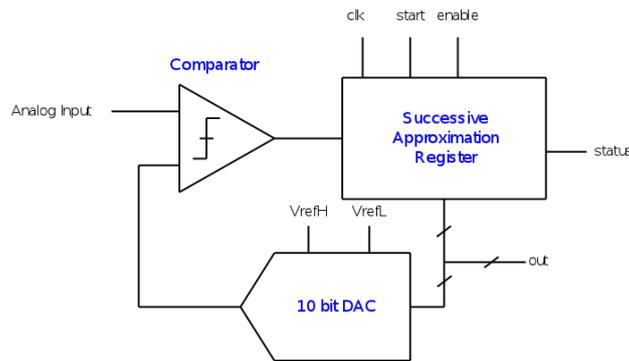
Since the Shunt-LDO regulator has no integrated voltage reference circuit, the reference volt-  
 age which defines the REG\_OUT voltage has to be provided externally (the FE-I4B has 4 refer-  
 1130 ence voltage outputs to choose from for this purpose). However biasing currents are generated by  
 an internal biasing circuit. The generated biasing voltage can be measured on the Vbp port. The  
 Shunt-LDO regulator requires an external capacitor of 2.2  $\mu$ F connected to the REG\_OUT port for  
 stable operation. In simulation, capacitors with an Equivalent Series Resistance (ESR) of about  
 1  $\Omega$  are recommended stable regulation, but on the as-built circuit, low ESR ceramic capacitors can  
 1135 be used without problems. The simulated output resistance of the regulators is significantly lower  
 than measurements of actual devices. This could be due to inaccuracy of the models, but is not  
 understood in detail.

### 4.13 Generic ADC

The GADC is a general purpose 10 bit Analog to Digital Converter designed for test and monitoring. It contains two main sub-blocks (Fig. 39): an input stage composed of an 8 to 1 analog multiplexer to select the input to convert, followed by a 10 bit ADC based on the Successive Approximation Register (SAR) architecture.



**Figure 39:** Block diagram of the EFUSE circuit

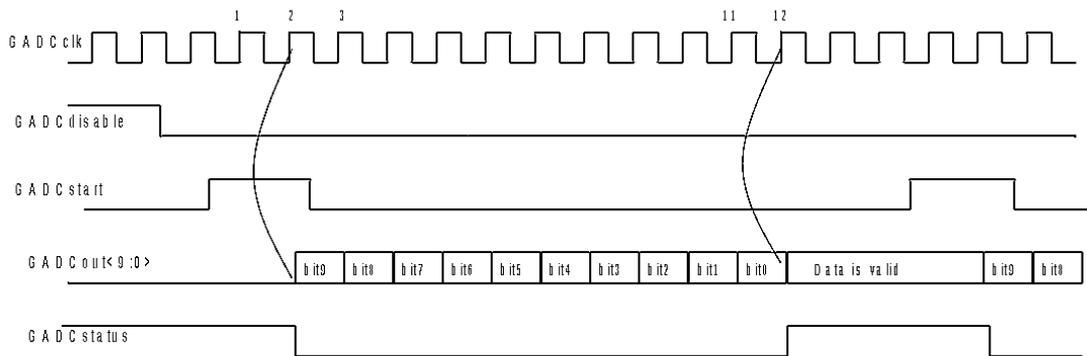


**Figure 40:** Block diagram of the EFUSE circuit

The GADCclk input clock frequency is the same as the main chip input clock which is typically 40 MHz. A 32:1 frequency divider is implemented in order to generate the internal clock driving the SAR ADC at 1.25 MHz. Level shifters are placed between logic gates working at 1.2 V and the others with 1.5 V as high level. This allows to drive correctly and safely the digital gates used inside the analog blocs.

The analog multiplexer has 8 sets of switches that connect analog inputs to a common output. A 3-bit address is decoded with combinatorial logic to select only one transmission gate to be in the ON state at any given time. Each transmission gate is built with a parallel combination of NMOS and PMOS transistors driven by a complementary gate. In this case the input signal is transmitted to the output without the threshold voltage attenuation. Low power (LP) transistors are used to minimize the effect of the leakage current.

The successive-approximation ADC is the most popular architecture for data-acquisition applications, especially when multiple channels require input multiplexing. The basic SAR architecture is shown in the Fig. 40. No input sample-and-hold stage is present in this design because input voltages are assumed DC or slowly varying signals. The conversion starts with the internal 10 bit DAC converter set to midscale. The comparator determines whether the input is higher or lower than the DAC output, and the result corresponding to the most-significant bit of the conversion is stored in the successive-approximation register respectively as a 1 or a 0. The DAC is then set either to 1/4 scale or 3/4 scale depending on the value of the MSB, and the comparator makes the decision for the second bit of the conversion. The result (1 or 0) is stored in the register, and the process continues until all of the bit values have been determined. At the end of the conversion process, a logic signal status is asserted. The internal DAC stage is based on a resistance network supplied through the reference voltage to generate the 10 bit voltage scaling. The integrated resistance area is chosen to keep the mismatch as low as possible and thus to achieve a high accuracy and linearity.



**Figure 41:** Block diagram of the EFUSE circuit

The timing diagram for the GADC is shown in Fig. 41. Each new conversion cycle is initiated by the input signal GADCstart. This signal does not need to be synchronized to the clock and the minimum needed duration is 1 clock cycle. On the second rising edge of the clock signal after the GADCstart has been set, the GADCstatus goes low and a new conversion starts. At the 12th clock cycle, the status turns low indicating the conversion is completed.

The ADC conversion accuracy depends heavily on the voltage reference stability. The GADCvrefHIGH is fixed via the Iout\_0 output current defined by a DAC (FEI4\_DACS\_ALL). An external decoupling capacitance of 47 nF connected to the pad GADCvrefHIGH is recommended in order to avoid the reference voltage variations during the GADC conversion cycle. In FE-I4B there s a wiring mistake such that GADCvrefHIGH is supplied by DAC already used for another function. It is therefore recommended to connect the GADCvrefHIGH bond pad to analog power.

The singals connected to the GADC inputs are defined in Table 12.

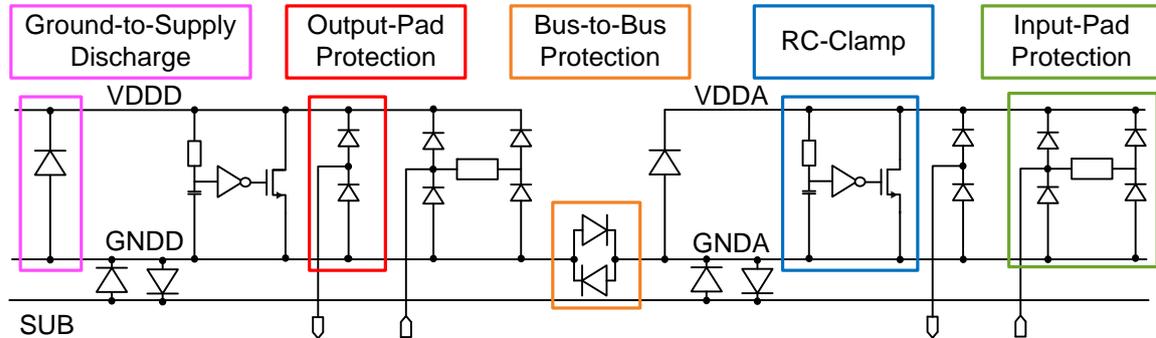
1180 **4.14 Temperature Sensor**

GADCsel code	Selected signal to digitize
0	Temperature sensor
1	GADC reference voltage- for testing
2	Analog ground- for testing
3	Analog MUX output, same as pad AnOut_P (see Sec. 5.4)
4	Analog regulator current sense Asens, $I \approx 1000 * (Asens/2k\Omega)$ .
5	10 bit DAC output (input to the calibration voltage pulser)
6	Half of regulated analog voltage
7	Ileak leakage current bus into 90 k $\Omega$ or 10 k $\Omega$ , depending on range bit (ILR)

**Table 12:** Selection of GADC inputs

## 5. Peripheral Circuits

### 5.1 ESD Protection



**Figure 42:** ESD strategy applied to the FE-I4 pad frame

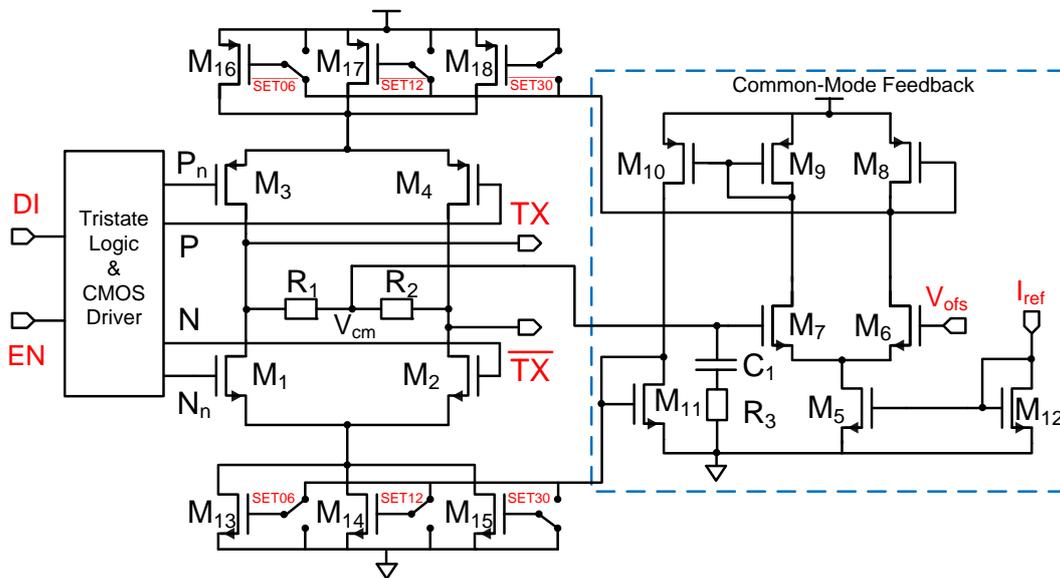
An ESD event is the abrupt discharge of static charge which is induced by human handling or contact with machines. An IC might get exposed to an ESD event during all phases of life-time starting with chip fabrication and extending to the various stages of assembly at system level and daily usage. In a typical work environment, a charged human body can lead to an electrostatic potential of up to 4000 V which during contact with a grounded object like an IC pin results in a discharge for about 100 ns with peak currents in the ampere range. Since the voltage levels that arise during an ESD event exceed the breakdown voltages of transistors and other components integrated on the chip, the implementation of a protection strategy is mandatory to avoid device destruction. The protection objective is to provide a discharge path of least impedance to ground through devices which have been designed to withstand large currents. During the discharge process the appearance of high voltage drops on the wires of the ESD network has to be avoided. High voltage drops would cause an ESD current flow into the sensitive internal circuits which would then be harmed.

The ESD protection strategy for the FE-I4 readout chip shown in Fig. 42 is based on recommendations of the process vendor. The applied strategy follows a non-self protecting approach which means that additional ESD devices are added in parallel to the I/O circuits. In case of the FE-I4 chip, the added ESD circuitry is formed by a double-diode network which connects the I/O pin to the supply rails by reverse biased diodes. During an ESD event of positive voltage the upper diode conducts a current to the positive supply rail while during an ESD event of negative voltage the current flows through the lower diode and originates from the ground bus. Due to the fact that the diode junction capacitance increases the capacitive load at the I/O pins, the diode dimensions have to be balanced between the demands for robust ESD protection and for high I/O circuit bandwidth. Input pads which provide connection to transistor gate electrodes are equipped with additional ESD structures to avoid the breakdown of the transistor gate-oxide during an ESD event. A series resistor and an additional secondary diode pair of smaller diode area is added to the primary double-diode network. The series resistor and the on resistance of the second diode pair form a voltage divider. Hence the voltage across the conducting diode of the primary diode network is reduced if the series resistor is higher than the on-resistance of the secondary diode pair.

1210 To provide an ESD current path from the positive supply voltage to the ground bus, an RC-triggered power clamp is connected between the supply rails. During normal operation the NMOS transistor of the RC-clamp circuit is switched-off whereas the NMOS transistor is switched-on during the transient pulse of an ESD event. ESD events can also induce a current flow into the ground pin. To avoid the current flow through parasitic diodes of the internal circuitry, dedicated  
 1215 ground-to-supply discharge diodes are added in parallel to the RC-clamp circuit. Since the diode junction capacitance is not harmful to the power supply bus, the diodes can be large without an impact on the chip performance.

The supply voltages of the FE-I4 chip are organized in several supply domains. In addition a dedicated ground rail is used for the definition of the substrate potential. Since an ESD discharge might cross the supply domain boundaries, it has to be avoided that the discharge happens through the connections which the internal sensitive circuitry has across the supply domains. For this  
 1220 reason a bus-to-bus protection circuit composed of an antiparallel connected diode pair is placed between the ground buses of the different supply domains and between the ground buses and the substrate rail which provides a discharge path of low impedance in both directions. Among others, the separation of the supply voltage into an analog and a digital domain is motivated by concerns  
 1225 related to crosstalk and noise. Due to the fact that the junction capacitance of the antiparallel connected diodes re-couples the supply rails to some degree, the choice of the diode dimensions is a trade-off between ESD reliability and isolation efficiency.

## 5.2 LVDS Driver



**Figure 43:** Schematic of the LVDS driver with common-mode feedback and adjustable signal current

1230 The LVDS driver shown in Fig. 43, has a standard circuit architecture adapted to lower supply voltages with the possibility of signal current magnitude adjustment. The driver implementation is based on the common four transistor switch scheme arranged in a bridge configuration. When

Ports	Type	Nominal Value	Description
vddLvds	Power	1.2 - 1.5 V	
vddT3	Power		T3 Well Isolation Voltage
gndLvds	Ground		
gndSub	Ground		Substrate Voltage
sub	Ground		Substrate
$I_{ref}$	Analog	60 $\mu$ A	Bias Current
$V_{os}$	Analog	vddLvds/2	Defined Offset Voltage
$V_{cm}$	Analog		Derived Common-Mode Voltage
TX		$I_{out} = \pm I_{06} + I_{12} + I_{30}$	Non-Inverted Signal Output
TXn		$I_{out} = \mp I_{06} + I_{12} + I_{30}$	Inverted Signal Output
DI	Digital		Data Input
EN	Digital		Enable Output Signal
SET06	Digital		Output Current Setting ( $I_{06} = I_{ref} * 10$ )
SET12	Digital		Output Current Setting ( $I_{12} = I_{ref} * 10$ )
SET30	Digital		Output Current Setting ( $I_{30} = I_{ref} * 30$ )

**Table 13:** LVDS driver Ports

DI	EN	N	Nn	P	Pn	Out
0	0	0	0	1	1	Z
1	0	0	0	1	1	Z
0	1	0	1	0	1	0
1	1	1	0	1	0	1

**Table 14:** Tristate-logic truth table

transistors M1 and M4 are switched-off and transistors M2 and M3 are switched-on, the polarity of the output current and in turn the polarity of the differential voltage is positive. In the inverted case, M1 and M4 are switched-on and transistors M2 and M3 are switched-off and the polarity of the output current is reversed. The choice of the dimensions of the switch transistors M1 - M4 corresponds to a trade-off between on-resistance and capacitive load for the CMOS drivers which generate the switch signals. A small on-resistance is desired to get a small voltage-drop across the switch transistors. This is important especially for small supply voltages due to the fact that the switch transistor voltage drop decreases the dynamic range of the differential and the common-mode signal. On the contrary, a small on-resistance is reached for wide transistor geometry which gives rise to larger capacitive load and increased power consumption. The transistor on-resistance has been chosen to generate a voltage drop of 50 mV for a signal current of 3 mA.

The common-mode voltage is sensed by means of a high ohmic voltage divider which is formed by resistors R1 and R2 of 100 k $\Omega$  each. The common-mode voltage is fed to the common-mode feedback circuit which compares the common-mode voltage with the applied offset voltage  $V_{os}$  by means of a NMOS differential pair. The biasing voltages of the NMOS transistors M13, M14, and M15 and the PMOS transistors M16, M17, and M18 are steered by the common-mode

feedback such that the applied offset voltage  $V_{os}$  is enforced. The common-mode feedback loop  
 1250 has been stabilized by a pole-zero compensation network formed by R3 and C1. For short-distance  
 communication, functionality has been added to decrease the magnitude of the signal current. By  
 setting configuration SET06, SET12 and SET30 bits, the gates of transistors M12-M14 can be  
 switched between the biasing voltage provided by transistor M11 and the ground potential while the  
 gates of transistors M15-M17 can be switched between the biasing voltage provided by transistor  
 1255 M8 and the supply voltage. For a bias current  $I_{ref} = 60\mu A$ , the output current is adjustable from  
 600  $\mu A$  to 3 mA.

A third high-ohmic state at the LVDS output is reached by opening all switching transistors M1  
 - M4 at the same time. The gates of transistors M1 - M4 are controlled independently by dedicated  
 signals P,Pn, N and Nn. A tristate logic block sets the signals at the gates of the switching transistors  
 1260 according to the truth table shown in Table 14 depending on the logic level of the enable (EN) and  
 the data input (DI) signal. The third high-ohmic state allows to multiplex data of several LVDS  
 drivers onto the same transmission line.

5.3 LVDS Receiver

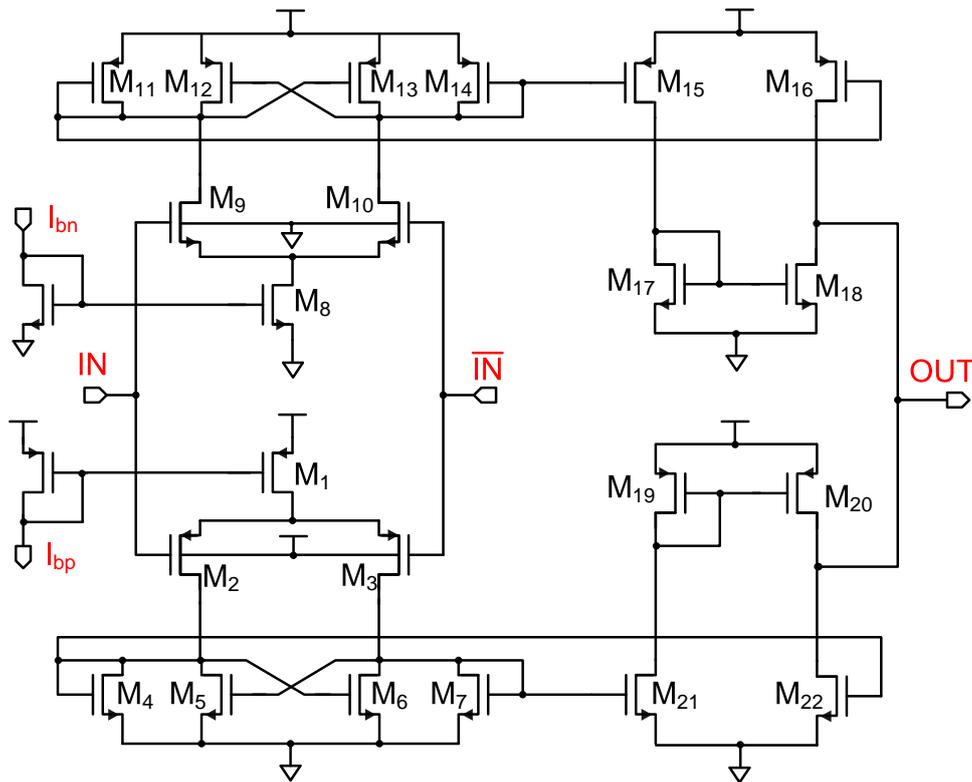
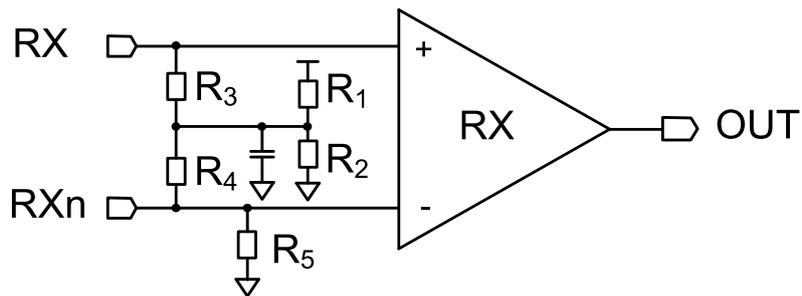


Figure 44: LVDS receiver with low voltage rail-to-rail input stage

The LVDS receiver implementation is shown in Fig. 44. An NMOS differential input stage  
 1265 and a PMOS differential input stage are connected in parallel to reach a wide range of input signal  
 common-mode voltages in which the LVDS receiver is capable to operate. For high input signal  
 common-mode voltages, the NMOS input stage is processing the input signal whereas the PMOS

input stage stops operating since the differential pair formed by transistor M2 and M3 drives the bias transistor M1 out of saturation. For low input signal common-mode voltages the PMOS input stage processes the input signal whereas the NMOS input stage stops operating since the bias transistor M8 is driven out of saturation. Both stages are equipped with a positive feedback decision circuit formed by transistors M4 to M7 and M11 and M14 which increases the switching speed and also allows the introduction of hysteresis. A high-gain second stage amplifier combines the two signal paths and converts the output signal to full-swing CMOS.

To reach a the wide input common-mode range, special care has been given to the choice of the threshold voltages of the differential input pair formed by transistors M2, M3 and M9, M10. The higher the threshold voltage of the NMOS differential pair transistors is, the smaller the input signal common-mode voltage region becomes in which the biasing transistor M1 remains in saturation. However, the smaller the threshold voltage of the NMOS differential pair transistors is, the smaller the region becomes in which the differential pair transistors M9 and M10 themselves stay in saturation. The process vendor provides transistor types with different threshold voltages which allows to have an optimal choice on the transistor threshold voltage. Due to the reverse short channel effect, the threshold voltage also varies with the channel length which has to be taken into account during transistor dimensioning. The smaller the channel length, the higher the effective threshold voltage becomes.



**Figure 45:** Fail-safe biasing circuit connected to the LVDS receiver input

Ports	Type	Nominal Value	Description
vddLvds	Power	1.2 - 1.5 V	
vddT3	Power		T3 Well Isolation Voltage
gndLvds	Ground		
gndSub	Ground		Substrate Voltage
sub	Ground		Substrate
$I_{bn}$	Analog	24 $\mu A$	Bias Current flows into NMOS
$I_{bp}$	Analog	-24 $\mu A$	Bias Current flows out of PMOS
RX			Non-Inverted Signal Input
RXn			Inverted Signal Input
Out	Digital		Data Output

**Table 15:** LVDS receiver ports

1285 An additional degree of freedom is introduced by the bulk-effect. In case the bulk and the source of a transistor are not connected to the same potential, the transistor threshold varies with the potential difference  $V_{SB}$  between source and bulk. The higher the potential difference becomes, the more the threshold voltage increases. As is shown in Fig. 44, the transistors of the differential input pairs have their bulk contact connected to the respective supply rail and not shorted to the source. As a result, the input transistors are subject to the bulk-effect. The source potential of the input transistors follows the voltage potential which is applied to the transistor gate and the threshold voltage is adapted dynamically to the common-mode voltage of the input signal. For example, in case of the NMOS input transistors, the threshold voltage decreases with decreasing input common-mode voltage which helps to keep the biasing transistor M8 in saturation. Furthermore, 1290 the threshold voltage increases with increasing input common-mode voltage which is beneficial to keep the NMOS input transistors M9 and M10 in saturation. 1295

Special attention has also been given to the propagation delay through the two signals paths corresponding to the NMOS and PMOS input stage. For a constant propagation delay independent of the input common-mode voltage, the propagation delays of both signal paths have to be equal. 1300 The propagation delay results from the time-constants defined by the transistor transconductance and the parasitic transistor capacitances. Due to the fact that NMOS transistors have an approximately four times higher mobility than PMOS transistors in this process, the  $W_P/L_P$  ratio of the PMOS transistors M11-M14 in the decision circuit has to be chosen four times higher than the  $W_N/L_N$  ratio of the NMOS transistors M4-M7 to reach the same transistor transconductance.

$$\frac{W_P}{L_P} = 4 \frac{W_N}{L_N} \quad (5.1)$$

1305 Moreover, since the oxide capacitance is equal for NMOS and PMOS transistors, the transistor area has to be equal so that an equal capacitive load results.

$$W_P L_P = W_N L_N \quad (5.2)$$

The conditions defined by 5.1 and 5.2 are met both by the following choice of transistor dimensions:

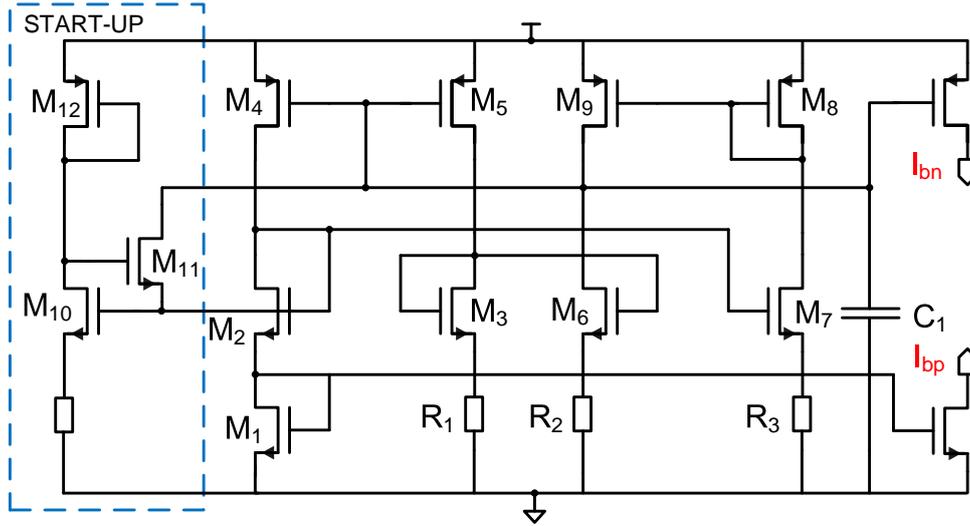
$$W_P = 2W_N \quad (5.3)$$

$$L_P = \frac{L_N}{2} \quad (5.4)$$

1310 Hence an equal signal propagation delay through both input stages results when the PMOS transistor width  $W_P$  is chosen twice the NMOS transistor width  $W_N$  and the PMOS transistor length  $L_P$  is chosen half the NMOS transistor length  $L_N$ .

### 5.3.1 Fail-Safe Circuitry

Under certain conditions, the CMOS output of the LVDS receiver might be undefined and reach an intermediate state of increased current consumption or even start oscillating. Such a condition can 1315 for example arise, if the LVDS receiver inputs are left open and are unused, if the LVDS driver is powered off, if the transmission line is broken or if the LVDS receiver inputs are shorted. To avoid



**Figure 46:** Low voltage biasing circuit with first order temperature compensation

that in any circumstance the LVDS receiver output settles to a undefined state, the device has to be equipped with a fail-safe circuitry.

The fail-safe circuit of the FE-I4 LVDS receiver is depicted in Fig. 45. A common-mode voltage of half of the supply voltage is generated by the voltage divider formed by the equally sized resistors R1 and R2. This voltage is fed to the LVDS receiver inputs by the two resistors R3 and R4 which are also of equal size. The differential voltage is generated by the pulldown resistor R5 which is connected to the inverting LVDS receiver input. The voltage difference between the two inputs is defined by:

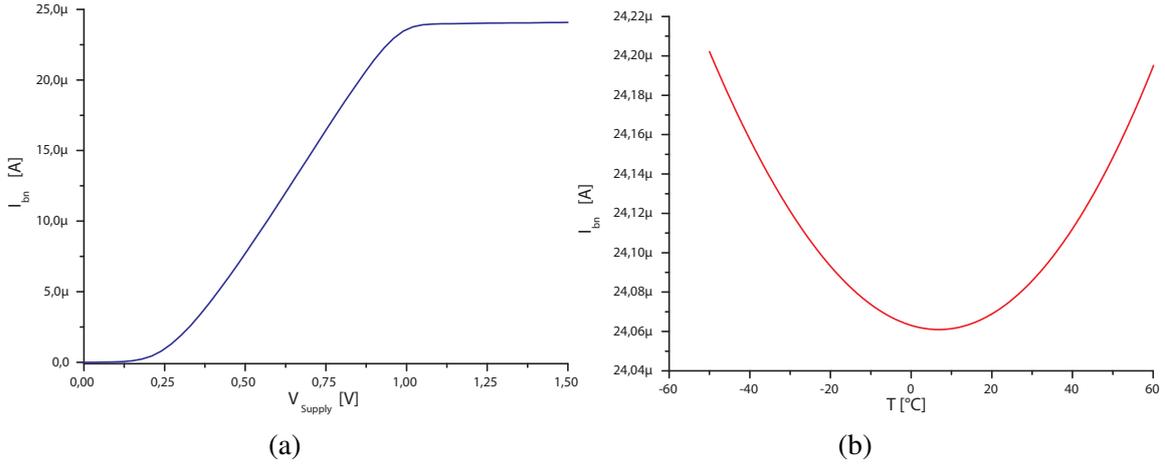
$$V_d = \frac{R_4}{R_1 + R_4 + R_5} V_{Supply} \quad (5.5)$$

The fails-safe circuit integrated on the FE-I4 readout chip generates a nominal differential voltage  $V_d$  of 60 mV. The chosen fail-safe scheme is far more robust to resistor mismatch with respect to traditional fail-safe circuits consisting of two resistive voltage dividers connected to each LVDS receiver input. In addition the used fail-safe architecture also addresses the scenario in which the LVDS receiver input pins are shorted. In case of a short, resistor R3 and R4 are connected in parallel which leads to a differential voltage which in fact is smaller than the voltage defined by equation 5.5 but still is high enough to enforce a defined output state.

### 5.3.2 LVDS Receiver Biasing

The biasing circuit of the FE-I4 LVDS receiver is shown in Fig. 46. The transistors M6, M7, M8 and M9 form a differential amplifier which senses the gate potential of the gate-drain connected transistors M2 and M3 and biases the transistors M4 and M5. The transistor M1 is introduced to reach a first order temperature compensation while resistors R2 and R3 are added to improve matching. The amplification loop enforces the same current through transistors M2, M3, M4 and M5 and resistor R1 and equalizes the gate potential of transistors M2 and M3. Kirchoff's voltage law gives:

$$V_{gs1} + V_{gs2} - V_{gs3} - IR_1 = 0 \quad (5.6)$$



**Figure 47:** Simulated LVDS bias current variation a) as a function of the supply voltage and b) as a function of the temperature

1340 Assuming that transistors M1, M2 and M3 are operating in strong inversion and applying a simplified square-law transistor model, equation can be written as:

$$\sqrt{\frac{2}{\mu C_{ox}} \frac{L_1}{W_1} I} + V_{th} - IR_1 = 0 \tag{5.7}$$

The temperature coefficient of the current I defined in equation 5.7 can be set to zero when the resistor  $R_1$  is chosen to be:

$$R_1 = \frac{V_{th}}{I} \frac{k_{\mu} + 2k_{th}}{k_{\mu} + 2k_{R1}} \tag{5.8}$$

1345 where  $k_{\mu}$ ,  $k_{th}$  and  $k_{R1}$  are the temperature coefficients related to the charge carrier mobility, the threshold voltage and the resistor R1, respectively. Both transistors M2 and M3 are gate-drain connected which gives a circuit configuration with a single high impedance node and simplifies stabilization. For stabilization, the capacitor C1 has been added to the  $V_{bias}$  port. The capacitance of C1 has been chosen such that a phase margin greater than  $60^{\circ}C$  is attained.

1350 To ensure that the biasing circuit reaches its nominal operating point when power is switched-on, the startup circuit composed of transistors M10, M11, M12 has been added. When no current flows through the transistors of the biasing circuit, the source potential of transistor M11 is close to ground and gate potential is close to the positive supply rail. The transistor M11 then enforces a current flow from transistor M9 through transistor M11 into transistors M2 and M1. When the nominal current point is reached, the source potential of transistor M11 increases whereas the gate potential decreases. As a result the transistor M11 is switched-off and does not influence the operation of the biasing circuit.

1360 As is seen from Fig. 47a, the biasing current settles at supply voltages higher than 1 V to a value of approximately  $24 \mu A$ . For supply voltages greater than 1 V, the biasing circuit has an output impedance of  $4 M\Omega$ . As is shown in Fig. 47b, the maximum variation of the biasing current in the temperature region of  $\pm 50^{\circ}C$  is about  $140 nA$  which corresponds to approximately  $0.5\%$  of the nominal current value. Monte-Carlo simulations give a standard deviation of  $1.3 \mu A$  when

process variation and component mismatch are taken into account which corresponds to 5% of the nominal current value.

Selected Column pair	Signal on analog output
0	Pixel (2,336) preamp output
1	Pixel (4,336) second stage output
2	Pixel (6,336) effective threshold voltage seen by the comparator
3	Pixel (8,336) preamp output
4	Pixel (10,336) second stage output
5	Pixel (12,336) effective threshold voltage seen by the comparator
6	Pixel (14,336) preamp output
7	Pixel (16,336) second stage output
8	Pixel (18,336) preamp output
9	Pixel (20,336) second stage output
10	Pixel (22,336) effective threshold voltage seen by the comparator
11	Pixel (24,336) preamp output
12	Pixel (26,336) second stage output
13	Pixel (28,336) effective threshold voltage seen by the comparator
14	Pixel (30,336) preamp output
15	Pixel (32,336) second stage output
16	Pixel (34,336) preamp output
17	Pixel (36,336) second stage output
18	Pixel (38,336) effective threshold voltage seen by the comparator
19	Pixel (40,336) preamp output
20	Pixel (42,336) second stage output
21	Pixel (44,336) effective threshold voltage seen by the comparator
22	Pixel (46,336) preamp output
23	Pixel (48,336) second stage output
24	Pixel (50,336) preamp output
25	Pixel (52,336) second stage output
26	Pixel (54,336) effective threshold voltage seen by the comparator
27	Pixel (56,336) preamp output
28	Pixel (58,336) second stage output
29	Pixel (60,336) effective threshold voltage seen by the comparator
30	Pixel (62,336) preamp output
31	Pixel (64,336) second stage output
32-63	Ground

**Table 16:** Signals on analog output depending on selected column pair address.

#### 5.4 Analog Output Buffers

1365 There is a single monitoring analog output at the bottom of the chip, on wire bond pad 1. Several  
signals are internally multiplexed onto this output. The multiplexing selection makes use of the  
same column pair selection used for pixel shift register access (see Sec. 7.2.1). The pad is inter-  
nally buffered and can be fed directly to an oscilloscope high impedance input or an active probe.  
1370 Table 16 shows the signal present on the multiplexed analog output depending on which column  
pair is selected. Refer to Fig. 4 for pixel numbering. Column pair mode does not affect this selec-  
tion. In addition to being present on the analog output, the multiplexed signal is routed to port 3 of  
the Generic ADC. This can be used to monitor DC levels, but obviously not to view the waveforms.

There are many additional test outputs at the top of the chip, as listed in the pinout table, but none of these will be accessible after a sensor has been bump bonded.

## 1375 6. Connection and Control

The primary method of communication with the FE-I4 chip is via a differential serial command input and a differential serial data output. An external differential clock, nominally 40 MHz, is required. The serial input is sampled on the rising edge of the clock. Alternate control paths through dedicated CMOS pins are also provided for test purposes. Prior to operating the FE-I4, 1380 certain physical connections must be made as described below.

### 6.1 Connection

The FE-I4B has functionality that must be enabled by making physical connections. This allows testing and debugging flexibility. This section describes only the connections needed for basic operation. A full pinout description is provided in the appendix. Only pads at the bottom of the 1385 chip are needed for basic operation. All power, ground and substrate pads at the bottom should be connected, as the horizontal power distribution within the chip is poor. Connections for using voltage regulators are given later. The following connections can or must be made regardless of how the chip is powered:

- 1390 • Chip ID (Cmd\_ChipId\_P<0>(??), Cmd\_ChipId\_P<1>(??), Cmd\_ChipId\_P<2>(??)): three wire bonds can be made to set the chip ID to something other than 000. This is not necessary for single chip operation, as there are internal pull-down resistors to default to 000 if the pads are left floating.
- 1395 • Current Reference (Iref\_out\_P(??), VbIn\_P(??)): this is the master current from which all other chip internal currents are derived. The chip outputs this current on pad Iref\_out\_P(??) which must be externally connected to pad VbIn\_P(??). By looping this critical current externally it is possible to substitute an external current source in case of problems and also to characterize the current reference as a standalone circuit.
- 1400 • Current reference trim (Iref\_trim[0-3]): the current reference is designed to produce  $2\ \mu\text{A}$  with good stability against temperature variations and radiation. However, the actual current will depend on the fabrication process parameters. Nominal parameters will indeed give  $2\ \mu\text{A}$ , but allowed parameter variations can result in 15% variance of the reference current. Four trim bits are provided to compensate for potential process variations. These pads must be wire bonded low or high as needed. They are internally pulled to the central value, so it is possible that there will be no need to bond them.
- 1405 • Resets (RA1bar\_P(45), RA2bar\_P(56), RD1bar\_P(88), RD2bar\_P(89)): all the resets are negative logic (i.e. ground means reset) and have internal pull-up resistors. Thus if left unbonded the chip should be functional. However, reset actions may be required, particularly upon applying power. RA1bar\_P(45) and RA2bar\_P(56) can be tied together to a common negative logic external signal, but RD1bar\_P(88) and RD2bar\_P(89) should remain separate. 1410 Alternatively, one can add an external capacitor to ground to implement an RC power on reset. All pads have internal pullup resistors.
- LVDS pads: Please see Section 6.2.

- GadcVref pad (43). It is recommended to connect this pad to VDDD (nominally 1.2V). See BufVgOpAmp and GADCVref in Appendix D.
- 1415 • Bypass control: all bypass control functions are internally pulled up or down to be normally off, thus ignoring all other pads should not interfere with operation. However, if one wishes to make use of alternate control pads and therefore wire bonds the SelCmd\_P(??) pad, care should be taken to hold this pin high for normal operation. It is internally pulled up in FE-I4B.
- 1420 • E-fuses: the programmable read only memory in the form of e-fuses is design to have some standalone capability so that the chip serial number can be retrieved even in the case of a damaged chip. It therefore has a separate power supply: VDDefuse(??). This pad should be connected to the same supply as VDDD1 for normal operation. Burning-in e-fuse value requires 3.3 V power as well as a dedicated low frequency clock and should only be done
- 1425 during wafer probing. Thus the pad VDD33(??) should never be wire bonded (it is a normal width pad because it must be contacted during wafer probing).

In case of using the voltage regulators to power the chip, the following connections must also be made:

- Adjustable reference voltages:
- 1430 • Fixed voltage reference:
- Shunt mode enable:

## 6.2 LVDS Pads

The FE-I4 differential inputs and outputs are compatible with the LVDS standard, but are not exactly conforming because they operate on a 1.2 V supply. These pads (listed below) are nevertheless referred to as LVDS. The LVDS driver and receiver circuits have been described in the circuit section. The LVDS receivers are self biased and will immediately work upon application of VDDD1. The LVDS output, on the other hand, must be enabled by writing the configuration memory.

- \* Aux\_Clk\_N(90) & Aux\_Clk\_P(91)  
An auxiliary clock input which can be selected for use by appropriate bit settings in the configuration memory. Not needed for normal operation.
- 1440 \* Ref\_Clk\_N(92) & Ref\_Clk\_P(93)  
The external clock input (normally 40 MHz). Required.
- \* CMD\_DCI\_N(94) & CMD\_DCI\_P(95)  
The serial command input. Required.
- 1445 \* DOB\_OUT\_N(104) & DOB\_OUT\_P(103)  
The serial output. Must be enabled before producing any output.

### 6.3 Commands

All configuration data between the ROD and the FE-I4 follow a simple serial command protocol. This protocol is subdivided in three major command classes, “Trigger”, “Fast”, and “Slow” commands. Due to the fact that we have a 40 MHz link between the ROD and the FE chip and trigger commands have to be passed to the chip without waiting, the FE-I4A has a Run Mode during which it will accept trigger and fast commands only and send back the corresponding hit data. If a slow command is received while the chip is in Run Mode the state machine will decode it but the CMD will send no internal control signals to the rest of the chip, and therefore slow commands other than “RunMode” will have no effect. In contrast, while in Configuration Mode the FE-I4A will process only slow commands (i.e. reset and configuration commands) but will not react to trigger or fast commands, as is the case with the present pixel detector modules. The chip can be placed in either Run Mode or Configuration Mode by issuing the “RunMode” slow command with the appropriate argument. Upon power-up or reset the chip will be in Configuration Mode.

In the Trigger command group the only command is “LV1”, in the Fast group there are three commands and in the Slow group there are six commands. Commands can have up to six different fields (numbered 1-6). All fields have fixed length with the exception of Field 6.

The possible values for the first two fields are listed in Table 17. Trigger and Fast commands have no further fields. Table 18 shows Fields 3-6 for Slow commands. A “-” for a field entry in the tables indicates that the field (and subsequent command fields) are ignored.

#### 6.3.1 Trigger & Fast Commands

Name	Field 1	Field 2	Description
size (bits):	5	4	
LV1	11101 <sup>1</sup>	-	Level 1 Trigger
BCR	10110	0001	Bunch Counter Reset
ECR	10110	0010	Event Counter Reset
CAL	10110	0100	Calibration Pulse
Slow	10110	1000	Slow command header

1: A single bit flip in the LV1 command will still result in a LV1 being decoded

**Table 17:** Trigger and Fast Commands

**LV1 (Trigger):** The LV1 command triggers the acquisition of a new event from the chip. This command simply generates a one clock wide pulse that is sent to the end of chip logic trigger input. Two or more consecutive trigger commands can be issued and will be decoded correctly. The minimum distance between two consecutive trigger *commands* is therefore five clock cycles. This is not to say that there can be no triggers on consecutive clock pulses, as the trigger count is multiplied in the EOCHL after receiving the command from the CMD. Any bit pattern resulting from flipping a single bit in the nominal pattern will still be interpreted as the original LV1 command with the correct timing. In addition to the LV1 command, a CMOS input to the chip permits supplying trigger pulses directly to the end of chip

logic from an external source. This external trigger input is ORed with any trigger pulses generated from LV1 commands.

**BCR** (Bunch Counter Reset): The bunch crossing counter inside the FE is set to zero in response to this command. It has no effect on any other internal structure. This command produces an output pulse of 1 clock cycle.

1480

**ECR** (Event Counter Reset): The ECR command is meant to completely clear the FE data path without touching the configuration of the chip. It can therefore be issued in order to synchronize events across the detector in case problems with data alignment are detected. This command resets and clears all memory pointers and data structures. This command produces an output pulse of 16 clock cycles.

1485

**CAL** (Calibration Pulse): In response to a CAL command a control pulse is sent to the internal Pulse Generator circuit. The Pulse Generator circuit then generates digital or analog calibration pulses and distributes them to the pixel array. This control pulse is user controllable by means of the 14 bits named CMDcnt stored in the configuration memory.

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CMDcnt[13:8] sets the delay, in clock cycle units, between the command detection and the beginning of the pulse. All values between 0 and 63 are allowed. Note that this is a digital coarse delay. A fine analog delay can be added by the Pulse Generator circuit, described separately.

CMDcnt[7:0] instead sets the width, always in clock cycles, of the calibration pulse that will be generated. The possible range is any value between 0 and 255; corresponding to pulse widths of one and 256, respectively.

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### 6.3.2 Slow Commands

The slow command is detected once the appropriate slow command header (10110 1000) has been found in the data stream. The fields following the header are interpreted according to Table 18.

1500

These fields are as follows:

- \* Field 3: This 4-bit field always exists and it defines the particular slow command.
- \* Field 4: This 4-bit field always exists and is the chip ID. The three least significant bits define the chip address and are compared with the geographical address of the chip (selected via wire bonding), while the most significant one, if set, means that the command is broadcasted to all FE chips receiving the data stream. If the chip ID does not match the geographical address of the FE or it is not a broadcast command, the command itself will be decoded but simply ignored.
- \* Field 5: This is the 6-bit address field. It holds the value of the address to be used with WrRegister or RdRegister commands. For the WrFrontEnd command this field is present but is ignored. Any value is fine but it is advisable to fill this field with 000000. In case of a GlobalPulse command the value written in this field is used to compute the width of the GlobalPulse pulse, which ranges from one to 64 clock cycles. In case of a RunMode command this field is used to toggle between RunMode (111000) and ConfMode (000111).

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1510



**RunMode** The chip has two modes which the command decoder can be placed in. There is a run mode, where the command decoder only acts on trigger and fast commands. There is also a configuration mode, where the command decoder only acts on slow commands. More concisely, the command decoder always processes the commands you send it, but depending on its mode it either does or does not produce output. This command toggles the FE between RunMode and ConfMode. In order to set the FE in RunMode one has to write 111000 in Field 5. A value of 000111 puts the chip in ConfMode. Any other combination of Field 5 does not change the RunMode status of the chip.

## 6.4 Test Pads

### 6.4.1 External Injection and Triggering

There are two test pads, ExtAnaInjectIn\_P(46) and ExtDigInjectIn\_P(50) which can be used for external analog and digital injection, respectively. Injection with either of these pads must be enabled by setting the configuration bits ExtAnaCalSW or ExtDigCalSW; these bits are located in global register 31.

Cmd\_ExtTrigger\_P(66) is a test pad capable of external triggering. Pulsing this high for 25ns will have exactly the same result as issuing a LV1 command through the command decoder. Sending the trigger in this method works regardless of the RunMode status of the command decoder itself; but no events or data will be sent to the user in response to the trigger if not in RunMode.

## 6.5 I/O Mux

The IOMUX block is a bank of multiplexed CMOS inputs and outputs provided for testing purposes. It has a 3-bit select field available as wire bond pads, which determines where the inputs and outputs are routed within the chip. There are four input pads (see Table 19) and three output pads (see Table 20).

Selected Block	IoMxSel_P [2:0] 67,68,69	IoMxIn_P				← bits ← pads
		[0] 70	[1] 71	[2] 72	[3] 73	
IoMx	000	LpBack	- <sup>1</sup>	-	-	
DOBT	001	DOBT_clk	DOBT_en	DOBT_se	DOBT_si	
EOCHLT	010	EOCHLT_tm	EOCHLT_si	EOCHLT_se	EOCHLT_ck	
Effuse	011	Effuse_RN	Effuse_CK	-	-	
SR	100	SRIN_FrmIoMx	SRCK_FrmIoMx	-	-	
CMDT	101	CMDT_SI	CMDT_CK	CMDT_SE	CMD_TM	
cReg	110	cRegSRClr	cRegLd	cRegClk	cRegDin	
abReg	111	abRegCKin	abRegDacLthClr	abRegSrclr	abRegDin	

1: Fields with “-” are not routed anywhere

**Table 19:** IOMUX Input

## 6.6 Programming the Shadow Registers

The shadow registers are alternate memory registers which are available to the user to bypass the normal configuration memory. However, only a selected subset of the global memory registers are shadowed (see Appendices C and D). The shadow registers are split into two independent structures, the abReg and the cReg. They consist of their own shift register and set of latches. Both can only be written to using bond pads, no commands are necessary. The abReg and cReg are implemented with slightly different features, although programming them is very similar. Most of the programming is done through the IOMUX, but there are some other dedicated pads required.

SelAltBus\_P(53) is a bond pad which determines if the chip should use the configuration memory or the shadow registers for configuration. Pulling SelAltBus\_P(53) high will give control of the chip to both these shadow registers; there is no option to only use one or the other. Pulling it low will give control of the chip to the configuration memory. SelAltBus\_P(53) is internally pulled low, but wire bonding to ground is recommended for normal detector operation. Toggling SelAltBus\_P(53) does not effect the elements of the configuration memory or shadow register. One can make use of this feature for rapid switching between two different configurations, for example to create power transients.

### 6.6.1 cReg

The cReg is 144 cells long. The user is able to clear its associated shift register, but not to clear the latches. Latches would need to be cleared by first having all zeros in the shift register, either by clearing or filling it explicitly with zeros, and then loading the latches. To fill the shift register, supply data at Din and feed it to the shift register with a clock provided at Clk. While you are supplying this clock, the old data will also be shifted out and can be viewed at SrOut. To load the latches from the shift register, pulse the Ld line high.

Selected Block	IoMxSel_P [2:0] 67,68,69	IoMxOut_P			
		[0] 78	[1] 79	[2] 80	← bits ← pads
IoMx	000	IoMxLpBack	1'b0 <sup>1</sup>	1'b0	
DOBT	001	DOBT_so	ErrorinBus[22]	ErrorinBus[23]	
EOCHLT	010	EOCHLT_so	EOCHLErrorOut1	CLK input to EOCHL	
Effuse	011	Effuse_srout	1'b0	1'b0	
SR	100	SRCK_OUTIoMx	SR_OUTIoMx	HitOr	
CMDT	101	CMDT_SO	1'b0	1'b0	
cReg	110	cRegSrOut	cRegOut143 <sup>2</sup>	cRegClkOut	
abReg	111	abRegSRout	bRegOut0 <sup>3</sup>	abRegCKout	

1: Fields with "1'b0" always return logical low.

2: cRegOut143 only when SelAltBus is high. Otherwise it is bit 15 of CNFGMEM register 31.

3: Always bRegOut0 regardless of SelAltBus.

**Table 20:** IOMUX Output

**1585 6.6.2 abReg**

The abReg is 288 cells long. It has the functionality to both clear the latches (DacLthClr) and its shift register (Srclr); to do either simply pulse the appropriate IOMUX input lines high. To fill the shift register, supply data at Din and feed it to the shift register with a clock provided at CKin. While you supply this clock the old data will also be shifted out and can be viewed at SRout.

1590 Once the shift register has been filled you then must load the latches. There are two bond pads regABstbld\_P(51) and regABDaclD\_P(52), which must be pulsed to load latches corresponding to the memories. The abReg actually controls two different subsets of global memory but shares a common shift register. Both of these pads control the latch loading for a different subset of latches in the abReg.

## 1595 7. Programming

The FE-I4 has wide functionality but a minimal command set. A sequence of several commands is typically needed to accomplish some meaningful action. This allows maximum flexibility, which means that the same action can typically be accomplished in several different ways. The best sequence to perform some action is given by the user needs and constraints, and by the performance to be measured. Some sequences may run “more smoothly” than others, and some, while logically possible, may not run at all. For example it will be logically possible to write all pixel registers in the entire chip at the same time, but because the chip is so large and writing a register produces a power transient, this may not work in practice.

### 7.1 Global Configuration

1605 The FE-I4 functionality is configurable by programming a master memory bank referred to as global registers (GR). It is necessary to program the GR in order to do anything meaningful. The GR also serves to retrieve non-hit information from the chip. The GR is organized as a random access memory of 16-bit words. Individual words are identified by 6-bit addresses. However, not all 64 possible addresses are used. Attempting to write an unused address will return an error message (but nothing bad will happen). The GR is accessed one register at-a-time via the WrRegister and RdRegister commands. The default settings for the programming of the GR are listed in appendix D. There is no clear command that will reset all registers to zero. However, such a reset does take place on power-up via an automatic power-on reset on the VDDA1 power supply, and it can be forced externally by pulling to ground both the RA1bar\_P(45) and RA2bar\_P(56) bond pads. Tables 21 and 22 summarize the register address allocation.

Address	Register Type	Function
0 - 31	Read/Write	Configuration of biases and operating settings
32 - 35	Read/Write with E-fuse PROM	Chip serial number and pixel SR repair

**Table 21:** Read/Write Registers

Address	Expected Return [15:0]
36-39	0000000000000000
40	00 + GADCout[9:0] + GADCStatus + GADCsel[0:2]
41	EventLimit[7:0] + 10101010
42	CMDerrReg[15:0]
43-63	0000000000000000

**Table 22:** Read-only Registers

In addition to the read and write register commands, the functionality of 27 out of the registers in the 0-31 range can be carried out by a completely separate, parallel structure, called the “bypass control”. The 432 bypass control bits are loaded as a stand-alone serial shift register, with the bits corresponding to GR 5 loading last and then transferred from this shift register to a shadow

1620 register that cannot be accessed in any other way (see section 6.6 for more information about programming the shadow registers). This bypass shadow register is completely independent from the GR. Reading GR registers cannot be used to find out what is in the bypass shadow register. Control of the chip can be given to the bypass register by pulling high the SelAltBus\_P(53) bond pad (if this pad is left floating it will be internally pulled low). Note that because the bypass register and the GR are completely independent, one may for test purposes have a different configuration in each one, and instantly switch between them by toggling the bypass control bond pad. This could for example be used to modulate current consumption for noise or power supply tests.

The E-fuse PROM allows burning in a unique serial number into each chip (see Appendix G) as well as a non-default selection bit for use of alternate pixel shift registers in selected double-columns, which can be useful to recover yield losses or failures. The GR with E-fuse PROM behave like normal registers, except that they “boot up” with the PROM values on power-up. They will also automatically reload the PROM values in case of an SEU (detected as a triple-redundant mismatch), or a re-load can be forced by issuing a “read E-fuse” pulse (using the GlobalPulse command). Burning of the PROM cannot be performed via commands, but only by applying a voltage of 3.3V and special control signals to dedicated bond pads. The value that is in the relevant GR will be burned in when such special signals are applied. Thus one must first load the desired values into the GR, read them back to verify that they were correctly stored, and only then apply the special signals to perform the burn-in. The default value of all E-fuses is 0, and burning a 1 is not reversible. Note, however, that the PROM values are not used for anything other than initializing the relevant GR, but the registers can be then changed with the WrRegister command like any other global register. In order to be certain of reading the PROM values (for example to retrieve the chip serial number) one should always issue a “read E-fuse” pulse before the RdRegister command. The PROM values can also be retrieved using a dedicated stand-alone shift register completely independent from the GR. This shift register has an independent power pin so that it should be readable even on a non-working chip as long as VDDD1 can be applied. VDDD1 is needed because direct access to the Efuse block is via the IOMUX pins (see Section 6.5), which are powered by VDDD1.

## 7.2 Pixel Configuration

### 7.2.1 Pixel shift register

1650 The pixel configuration is single column-pair oriented. One can think of the chip as having only one 672-pixel double-column: this is the length of the pixel shift register. The pixel shift register is written by the WrFrontEnd command. If the SRRead bit in the GR configuration is set while issuing a WrFrontEnd command, 672 bits are sent to the chip output. These are typically the bits that were previously in the shift register. There is no separate read shift register command. The pixel registers themselves are not affected by the WrFrontEnd command. To program the pixel registers, data must be copied from the shift register to the appropriate latches as explained later. This must be done by the user with a sequence of commands in addition to WrFrontEnd (or even without the WrFrontEnd command in case of special cases such as writing the same value into all pixels of a double-column).

1660 In reality the chip has 40 double-column's, each one with an identical 672-bit shift register. The WrFrontEnd command writes to none, one, or several of these 40 double-columns in parallel, as determined by the PxSRSEL GR. This contains a 2-bit mode (Colpr\_Mode) and a 6-bit address (Colpr\_Addr) that can be 0-39 for the double-column number. Values higher than 39 are also supported. Table 23 indicates which double-columns are selected depending on the mode and  
1665 address.

Colpr_Mode	Action
00	Write only the addressed DC
01	Write every 4 <sup>th</sup> DC with such phase as to include addressed DC
10	Write every 8 <sup>th</sup> DC with such phase as to include addressed DC
11	Write all DCs

**Table 23:** Selection Modes of the Double-columns

Colpr_Addr	Action
0-39	Read the given double-column
40, 48-55	Grounded
41-47, 56-63	Loop-back(Read the input to the shift register instead of the output). Normally no need to use these values.

**Table 24:** Read-back action depending on column address values

The double-column selection not only affects the shift register, but also other analog column operations such as transfer of bits from shift register to pixel registers and vice-versa, or HitOR output enable. It does not affect the digital column enabling, for which there is a dedicated mask. For all modes the shift register of the addressed double-column is read back during the write operation.  
1670 If the address >39 then the input bit stream may be looped back or a fixed value sent to the readout as shown in Table 24. Thus, for example, Colpr\_Addr=18 (decimal) and Colpr\_Mode=10 (binary) will write double-columns 2, 10, 18, 26, and 34 and at the same time read back double-column 18, while Colpr\_Addr=42 and Colpr\_Mode=10 will write the same group of 5 double-columns but will copy the input bit stream directly to the output instead of reading back any of them.

1675 Finally, the WrFrontEnd command will not unconditionally transfer a 672-bit stream to the selected pixel shift registers, because the shift register has several operating modes, controlled by the global configuration bits S0, S1, and HitLd (Table 25). It is up to the user to ensure that the shift register is in shift mode (S0=S1=HitLd=0) before issuing the WrFrontEnd command.

1680 The WrFrontEnd command for a given double-column will fill the pixel shift register such that the last row of the lower-numbered column is filled last, see Figure 4. For example, in double-column 0 (columns 1 and 2), the last pixel filled is 1, 336. For double-column 20 (columns 41 and 42), the last pixel filled is 41, 336.

### 7.2.2 Calibration Pulse Injection

The PxSRSEL GR mentioned earlier has a 2-bit mode (Table 23) and a 6-bit address (Table 24). The

1685 selection of the double-columns for calibration pulse injection is different for analog injection and digital injection.

### Digital Injection

The digital injection is straightforward. The 6-bit Colpr\_Address which can be 0-39 corresponds to double-columns indicated by this formula:

1690 If Colpr\_Addr is  $n$ , the columns selected will be  $2n + 1$ , and  $2n + 2$ .

Thus Colpr\_Addr=0 corresponds to columns 1 and 2. Colpr\_Addr=5 corresponds to columns 11 and 12 and Colpr\_Addr=39 corresponds to columns 79 and 80. Recall that while column pair numbering starts at 0, column numbering starts at 1 (see Section 3). In addition, to perform digital injection DIGITIN\_SEL (which is in GR 21) must be set high.

### 1695 Analog Injection

For analog injection, the 6-bit Colpr\_Addr (values 0-39) is translated into single column selection as follows :

Colpr\_Addr=0 corresponds to single column 1 only. Colpr\_Addr=39 corresponds to the triplet of columns 78, 79 and 80. For all other addresses, the two columns selected are:

1700 If Colpr\_Addr is  $n$ , then the columns selected are  $2n$ , and  $2n + 1$ .

Thus, Colpr\_Addr=1 corresponds to columns 2 and 3, Colpr\_Addr=5 corresponds to columns 10 and 11.

The modes described in Table 23 work in the same way as described earlier. For example, Colpr\_Addr=10 (decimal) and Colpr\_Mode=10 (binary) will select column pairs 2, 10, 18, 26, and 34 and thus the columns which correspond to those double-columns based on the respective formulas for digital and analog injection.

1705

## 7.2.3 Pixel SEU hard registers

Each pixel has 13 SEU hard transparent latches. These can be set to either latched or transparent for a whole double-column at once. Thus, in a given double-column, all bit 0 latches can be either latched or transparent at the same time. For a latch to be transparent three things have to happen:

1710

S0, S1, HitLd <sup>1</sup>	Description
0,0,0	Normal shift mode; shifts in on clock rising edge and out on falling edge
1,0,0	Clock rising edge loads "1" in parallel into all cells
0,1,0	Clock rising edge loads "0" in parallel into all cells
1,1,0	Clock rising edge loads selected <sup>2</sup> pixel register value into all cells in parallel
0,0,1	Shifts in on clock rising edge and out on falling edge
1,0,1	Clock has no effect. Comparator rising edge sets bit for each pixel
0,1,1	Clock rising edge loads "0" in parallel into all cells
1,1,1	Clock has no effect

1: Effects of HitLd = 1 modes are not well understood and are best to be avoided except when used for hit flagging (see Section 8.6).

2: For how pixel register cells are selected see Section 7.2.3

**Table 25:** Shift Register Modes

(1) the corresponding pixel strobe bit must be set in the PxStrobes GR, (2) the double-column in question must be selected (see previous section), and (3) an internal signal called LatchEn must be high. The LatchEn signal cannot be set to static high. It can only be pulsed high using the Global Pulse command with the LatchEn bit in GR 27 set to 1. This seemingly complex scheme was designed to be very tolerant of SEUs not only in the latches themselves but also in the logic that controls the programming of the latches. There is no reset or clear command for the pixel latches - they can only be cleared by writing the value zero.

Unlike the LatchEn signal, any combination of pixel strobe bits can be set to static high as desired. The pixel strobe bits control not only which latches can be written, but also which ones can be read back. To read back a given latch, the inverse of the value in the latch must first be transferred to the shift register cell of every pixel in the double-column (using S0=S1=1), and then shifted out using the WrFrontEnd command with SRRead set to 1. It is important to note that read-back has negative logic: what is read back is the negative of what is stored! This was done because the layout turned out to be slightly more compact than for positive logic. Since the shift register has only one bit per pixel, only the inverted value from one of the 13 latches can be transferred to the shift register at a time. This will be the lowest order pixel latch that is set. Thus if the pixel latch for bit 0 is set, then bit 0 inverse will be read out regardless of what other latches are set.

PxStrobes	Latch controlled in the pixel
[0]	Output enable. Must be set to 1 to see hits through the normal readout path.
[1:5]	TDAC value [1]=MSB
[6]	Large injection capacitor. Must be 1 to inject charge through this capacitor.
[7]	Small injection capacitor. Must be 1 to inject charge through this capacitor. In parallel with large capacitor.
[8]	Imon and Hitbus out. Must be 1 to monitor leakage current or 0 to include pixel in hit bus.
[9:12]	FDAC value [12]=MSB
SR <sup>1</sup>	Enable digital injection

1: The shift register (SR) bit in each pixel is “overloaded” with the function to enable digital injection, in addition to its primary function of being the data input to the latches

**Table 26:** Pixel Latch Assignments

### 7.3 Examples

This section provides command sequences to perform some common pixel register operations. It may be possible to achieve the same result with different command sequences. Specific GR or bits within GR are identified by functional names rather than register numbers. The name-to-number assignment is provided in appendix C.

### 7.3.1 Clear the pixel shift register

Table 27 provides the command sequence needed to clear the shift register (set all bits to 0).

	Issue command	To do what	Comments
1	WrRegister (GR 22)	Select DC(s) for operations	
2	WrRegister (GR 13, 21)	Set S0=S1=HitLd=0	Set SR in normal mode
3	WrRegister (GR 27)	Set SRClr=1	Set SRClr, de-select all others
4	GlobalPulse	Pulse SR clear line	Clears the SR of selected DCs

**Table 27:** Commands to clear the shift register.

### 1735 7.3.2 Set all pixel shift register bits to 1

The pixel shift register cells have a clear function but not a set function. However, all the bits can be set to 1 simultaneously by changing the operating mode from normal shift to parallel input. This is done with GR bit S0 and issuing a single clock pulse to the shift register as described in table 28.

	Issue command	To do what	Comments
1	WrRegister (GR 22)	Select DC(s) for operations	
2	WrRegister (GR 13, 21)	Set S0=1, S1=HitLd=0	Sets SR in parallel input mode
3	WrRegister (GR 27)	Set SR_Clk=1	Set SR_Clk, de-select all others
4	GlobalPulse	Pulse SR clock line	Clocks SR to latch in 1s
5	WrRegister (GR 13, 21)	Set S0=S1=HitLd=0	Return SR to normal mode

**Table 28:** Commands to set all the shift register bits to 1.

### 7.3.3 Load arbitrary bit stream into pixel shift register and read back previous contents

1740 There is a direct command to do this, but recall that the command structure is single double-column oriented: the write command thinks there is only one shift register 672 bits long. The full chip is accessed by repeating the same operation on different sets of double-columns by changing the PxSRSel GR. The same sequence is used to put a new bit stream into the shift register and to read back what was there before, but note that writing can happen to multiple double-columns in parallel  
1745 (depending on PxSRSel mode), but only 1 of those double-columns is read back. The configuration bit SRRead has to be set to 1 in order for the shift register content to be presented at the chip output. Table 29 shows the command sequence.

### 7.3.4 Load pixel latches

1750 The only two possible operations on the pixel latches are load and read. There is no command to reset latches to zero, because such functionality would make the latches vulnerable to SEUs. However, all latches will initialize to zero on power-up, and re-initialization can be forced externally by pulling down both the RA1bar\_P(45) and RA2bar\_P(56) bond pads simultaneously. Table 30 provides the command sequence needed to copy the shift register contents into 1 or more pixel latches.

Issue command	To do what	Comments
1 W <sub>r</sub> Register (GR 22)	Select DC(s) for operations	
2 W <sub>r</sub> Register (GR 13, 21)	Set S0=S1=HitLd=0	Sets SR in normal mode
3 W <sub>r</sub> Register (GR 27)	Set SRread=1	Needed to read back SR
4 W <sub>r</sub> FrontEnd	Clocks 672 bits in	672 bits are sent out

**Table 29:** Commands to load an arbitrary bit stream to the shift registers.

Issue command	To do what	Comments
1 W <sub>r</sub> Register (GR 22)	Select DC(s) for operations	
2 W <sub>r</sub> Register (GR 13, 21)	Set S0=S1=HitLd=0 and P <sub>x</sub> Strobes bits for latch to load	
3 W <sub>r</sub> Register (GR 27)	Set LatchEn=1	Set LatchEn, de-select all others
4 GlobalPulse	Pulse LoadLatches line	Copy SR bits to selected latches
6 W <sub>r</sub> Register (GR 13)	Set all bits to 0	Bad for SEU to leave strobe bits high

**Table 30:** Commands to load the shift register content to the pixel latches.

### 1755 7.3.5 Copy inverse of pixel latch contents to pixel shift register

This is the only way to read back pixel latches. First the latch contents must be copied into the shift register, and then the shift register must be read out. Note that the latch contents are inverted when transferred back to the shift register. The latch corresponding the lowest value P<sub>x</sub>Strobe bit is copied to the shift register. The necessary command sequence is given in Table 31.

Issue command	To do what	Comments
1 W <sub>r</sub> Register (GR 22)	Select DC(s) for operations	
2 W <sub>r</sub> Register (GR 13, 21)	Set S0=S1=1, HitLd=0 and P <sub>x</sub> Strobes bit for latch to copy	Sets SR in parallel input mode and select the latch to copy
3 W <sub>r</sub> Register (GR 27)	Set SR_Clk=1	Set SR_Clk, de-select all others
4 GlobalPulse	Pulse SR clock line	Clocks SR to copy the selected latch
5 W <sub>r</sub> Register (GR 13, 21)	Set S0=S1=HitLd=0	Return SR to normal mode

**Table 31:** Commands to copy pixel latch contents to pixel shift register

### 1760 7.3.6 Perform calibration pulse injection

FE-I4 features an internal pulse generator circuit to perform digital or analog injection to the pixels even when no sensor is connected. See section 8.2 for how to calibrate the pulser. In RunMode, the CAL command can be used to send the injection pulse to the pixels. Table 32 gives the command sequence to perform digital injection using the CAL command and table 33 gives the commands for analog injection with the CAL command. When not in RunMode, calibration injection can be

performed using the GlobalPulse command, see table 34 for digital injection and 35 for analog injection.

	<b>Issue command</b>	<b>To do what</b>	<b>Comments</b>
1	WrRegister (GR 22)	Select DC(s) for operations	
2	WrRegister (GR 13, 21)	Set S0=S1=HitLd=0 and select output enable in PxStrobes	Sets SR in parallel input mode and selects enable latch
3	WrFrontEnd	Write 1 to selected pixels	
4	WrRegister (GR 27)	Set LatchEn=1	Set LatchEn, de-select all others
5	GlobalPulse	Pulse LoadLatches line	Copies SR bits to latches, leave 1s in SR
6	WrRegister (GR 13)	Set all PxStrobes bits to 0	
7	WrRegister (GR 21)	Set DIGHTIN_Sel=1	Enable digital injection
8	WrRegister (GR 26)	Set CMDCnt	Set delay and width of injected pulse
9	RunMode	set the chip in RunMode	
10	CAL	Send injection pulse to selected pixels	

**Table 32:** Commands to perform digital injection using the CAL command.

	<b>Issue command</b>	<b>To do what</b>	<b>Comments</b>
1	WrRegister (GR 22)	Select DC(s) for operations	
2	WrRegister (GR 13, 21)	Set S0=S1=HitLd=0, select output enable, small/large capacitance in PxStrobes	Sets SR in parallel input mode and selects enable and cap latch
3	WrFrontEnd	Write 1 to selected pixels	
4	WrRegister (GR 27)	Set LatchEn=1	Set LatchEn, de-select all others
5	GlobalPulse	Pulse LoadLatches line	Copies SR bits to latches
6	WrRegister (GR 13)	Set all PxStrobes bits to 0	
7	WrRegister (GR 22)	Select DC(s) for analog injection	see section 7.2.2 for addressing of analog injection
8	WrRegister (GR 26)	Set CMDCnt	set delay and width of injected pulse
9	RunMode	set the chip in RunMode	
10	CAL	Send injection pulse to selected pixels	

**Table 33:** Commands to perform analog injection using the CAL command.

Issue command	To do what	Comments
1 WrRegister (GR 22)	Select DC(s) for operations	
2 WrRegister (GR 13, 21)	Set S0=S1=HitLd=0 and select output enable in PxStrobes	Sets SR in parallel input mode and selects enable latch
3 WrFrontEnd	Write 1 to selected pixels	
4 WrRegister (GR 27)	Set LatchEn=1	Set LatchEn, de-select all others
5 GlobalPulse	Pulse LoadLatches line	Copies SR bits to latches, leave 1s in SR
6 WrRegister (GR 21)	Set DIGHITIN_Sel=1	Enable digital injection
7 WrRegister (GR 13)	Set CalEn=1	Set CalEn, de-select all others
8 GlobalPulse	Send injection pulse to selected pixels	

**Table 34:** Commands to perform digital injection using the GlobalPulse command.

Issue command	To do what	Comments
1 WrRegister (GR 22)	Select DC(s) for operations	
2 WrRegister (GR 13, 21)	Set S0=S1=HitLd=0, select output enable, small/large capacitance in PxStrobes	Sets SR in parallel input mode and selects enable and cap latch
3 WrFrontEnd	Write 1 to selected pixels	
4 WrRegister (GR 27)	Set LatchEn=1	Set LatchEn, de-select all others
5 GlobalPulse	Pulse LoadLatches line	Copies SR bits to latches
6 WrRegister (GR 22)	Select DC(s) for analog injection	see section 7.2.2 for addressing of analog injection
7 WrRegister (GR 13)	Set CalEn=1	Set CalEn, de-select all others
8 GlobalPulse	Send injection pulse to selected pixels	

**Table 35:** Commands to perform analog injection using the GlobalPulse command.

## 1770 7.4 Scan Chain

All the scan chains are accessed in the IOMUX interface (See Section 6.5) and are implemented for the data output block, end of chip logic, and command decoder. All of the scan chains for a given block are the same length:

- DOB - 72 bits
- 1775 · EOCHL - 3192 bits
- CMD - 262 bits

## 8. Data Acquisition

After the FE-I4 has been configured (see Section 7) it should be put into RunMode for data acquisition. Four types of RunMode data acquisition are possible: external trigger, calibration, self trigger, and stop mode. Only fast commands are possible when in RunMode: trigger (LV1), calibration pulse (CAL), bunch counter reset (BCR), and event counter reset (ECR). Additional “slow” data acquisition modes are possible using alternate output pads. The HitOr\_P(105) pad is a wired OR of all selected pixels, and thus can be used to detect hits in real time without knowing which pixel they came from (unless only one pixel is enabled. Additionally, by setting the HitLD configuration bit, the pixel configuration shift register can be used as data output buffer to record whether each discriminator fired or not (without knowing how many times it fired).

### 8.1 External Triggering

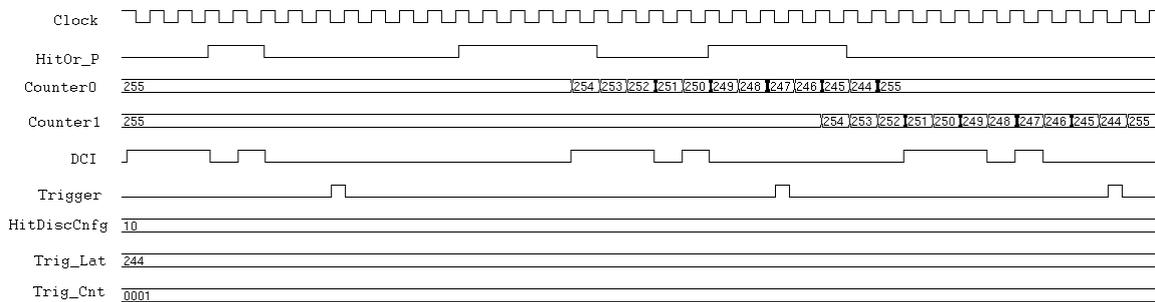
This acquisition mode is appropriate for reading hit data from a detector with an external trigger system. It is the mode that will be used in the running experiment and in beam tests. All enabled pixel regions will automatically store events upon detection of a big hit without any user intervention (recall that a big hit is a discriminator pulse exceeding the programmed HitDiscCnfg. See Table 7). The leading edge of a big hit pulse starts an 8-bit latency counter within the hit region. The counter starts at 11111111 (decimal 255) and counts down with the system clock, until it reaches the Trig\_Lat value programmed in the chip configuration memory. Note Trig\_Lat is *not* the actual value of the trigger latency, but its 8-bit complement. Thus if a trigger latency of 120 clocks is desired ( $120 \times 0.025 = 3 \mu\text{s}$ ), one must program a Trig\_Lat value of  $255 - 120 = 135$ .

When the chip recognizes a trigger command, a burst of trigger pulses is sent in parallel to all the regions. The length of this burst is given by the programmed trigger multiplier value TrigCnt, which can be 0 to 15. The value 0 produces a 16 pulse burst. The pulses in the burst are spaced by one clock. A LV1 trigger (positive pulse) can also be supplied directly on the Cmd\_ExtTrigger\_P(66) input pad. Internally a burst will be produced exactly as before. Note that the LV1ID should be disregarded when using external injection as the counters are not reliable when using external triggering. Issue an ECR command to reset the LV1ID counter when returning to command oriented triggering (if necessary). External triggering also works regardless of the RunMode status of the chip.

For a hit region to be selected for read out, a trigger pulse must reach the region while one of the region’s five latency counters is equal to Trig\_Lat. For each latency counter, if no trigger pulse arrives while this condition is true, the next clock cycle both resets the counter to 255 and clears the corresponding ToT data within the region. A Trig\_Lat value of 255 is not supported and the user should not expect for the triggering to function properly.

An example timing diagram is given in Figure 48. In this example the trigger latency is set to 244, the trigger multiplier is set to one, and HitDiscCnfg is set to 2. The first pulse on HitOr\_P(105) is from a hit which is smaller than HitDiscCnfg and is thus not saved; no latency counter is enabled and the trigger does nothing. The second and third injections are considered big hits and therefore you can see a latency counter begin for each injection. The second trigger does not land on Trig\_Lat and thus has no effect. You can then see the latency counter count down to Trig\_Lat and eventually reset itself. The third trigger is a successful one (hit data comes out from the chip) as it occurs

exactly at Trig\_Lat. Please note that this diagram is from a real simulation using external injection to inject the hits and commands for everything else.



**Figure 48:** Proper Latency and Trigger Timing Example

1820 The chip can queue a maximum of 16 triggers for readout at any given time. Commands that  
 overflow this buffer will result in skipped triggers (see Section ??). The chip must be in RunMode  
 the entire time that trigger pulses are being generated. It is not enough that the LV1 command itself  
 was issued while in RunMode. For example, if the trigger multiplier is set to 15 and the user exits  
 RunMode immediately after issuing a LV1 command, only a fraction of the expected 15 triggers  
 1825 will actually be sent to the columns.

## 8.2 Calibration

Even without a sensor connected, hits can be produced in pixel regions by either digital or analog injection. There are many different ways to produce injection pulses, but generally can be classified as using the internal pulse generator block, or not.

1830 The internal pulse generator block can be thought of as a typical benchtop pulse generator  
 instrument, with a trigger input, a programmable delay, and both analog and digital output pulses.  
 The term “start input” will be used here instead of “trigger input” to avoid confusion with the chip  
 trigger function. Not only the leading edge, but also the width of pulses provided to the start input  
 have meaning. Start pulses can be generated by issuing a CAL command if in RunMode, by issuing  
 1835 a control pulse command if not in RunMode, or by directly supplying to the Cmd\_AltPls\_P input  
 pad with the appropriate configuration regardless of RunMode. The latter two methods require the  
 chip to have been configured to route the command pulse to the pulse generator (see Section 7.3.6).  
 The relationship between the start input and the digital and analog outputs is shown in Figure 49.  
 The delay and analog output level are programmable. The return to programmed level of the analog  
 1840 output uses a slow ramp (also programmable) to avoid wrong polarity charge injection. The falling  
 edge of the analog output produced negative charge injection (the correct polarity for pixel amplifier  
 input).

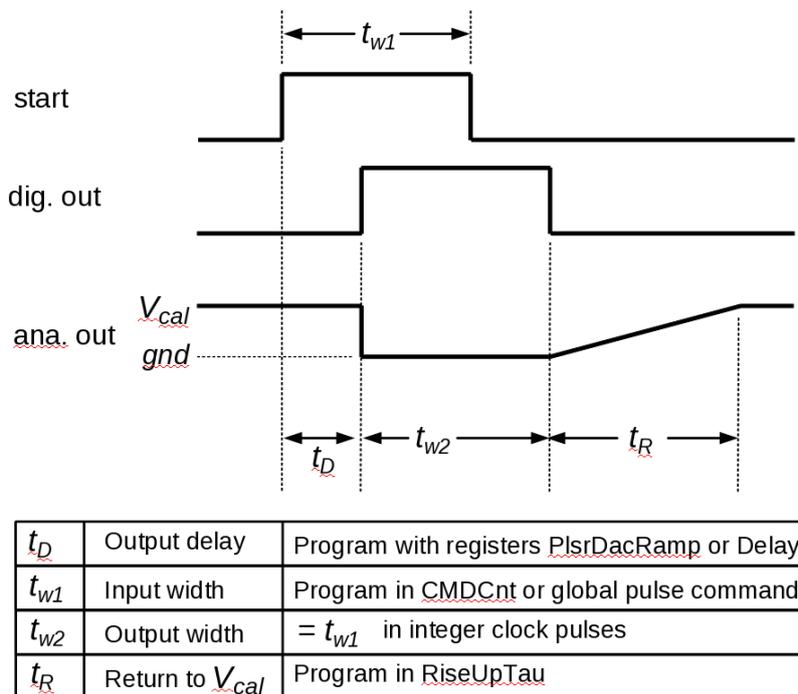
Analog or digital injection can also be accomplished without using the pulser. An external  
 positive digital pulse can be supplied to pad ExtDigInjectIn\_P(50) for digital injection (note that  
 1845 the ExtDigCalSW bit must be set for this to work). An external negative edge (voltage should  
 always be between ground and VDDA1) can be supplied to pad ExtAnaInjectIn\_P(50) for analog  
 charge injection (note that ExtAnaCalSW bit must be set for this to work).

The digital injection pulse can be routed in parallel to any set of pixels by (1) enabling digital injection by setting the DIGITIN\_SEL configuration bit, (2) selecting the column pairs for injection using the Colpr\_Mode and Colpr\_Addr registers, and (3) loading a 1 into the shift register for all desired pixels (zero for all not desired pixels) of the enabled columns (see section 7.3.6). All three conditions are required. The digital injection pulse is ORed with the comparator output. Therefore, the analog state must be “below threshold”, or the discriminator must be off (bias current set to zero) for digital injection to work. For example, setting a very low discriminator threshold with the comparator active will prevent digital injection from working, because the discriminator will be always high. The width of the digital injection pulse will simulate the time over threshold response.

The analog injection pulse can be routed in parallel to any set of pixels by (1) selecting the column pairs for injection using the Colpr\_Mode and Colpr\_Addr registers, and (2) setting the injection capacitor pixel configuration bits of the desired pixels in the enabled columns (see section 7.3.6). There are two switchable injection capacitors, one much larger than the other, that can be used in any combination (see section 4.2).

The injection techniques described above allow the user to populate pixel regions with hits at will. The external trigger methods can then be used to produce output in the usual way. It is up to the user to determine the correct timing of LV1 commands or other triggers relative to CAL commands or other injection methods.

If the user is injecting a hit, and the injection pulse width is sufficiently large such that a trigger



**Figure 49:** Outputs of pulse generator circuit block relative to start input. The analog output level,  $V_{cal}$ , can be programmed with register PlsrDAC.

pulse is sent to the columns while still injecting the trigger will be ignored. For example, if there is an injection lasting 20 clock cycles using a CAL command but the user only waits 10 clock cycles before issuing the trigger then the trigger will not be accepted by the PDR. This is because the trigger would occur 10(user wait) + 5(clock cycles needed to issue LV1 command) after the end of the CAL command but the injection is still occurring.

### 8.2.1 Pulser Configuration

The parameters of the pulser are configurable for maximum flexibility, but this also means they must be properly programmed before the pulser can be used. Referring to Fig. 49, the Vcal DC voltage level, the  $t_D$  delay, and the  $t_R$  rise time must be programmed. The Vcal voltage generation requires a bias to be programmed as well as the voltage itself. The delay is programmed with a combination of a current and a ratio (2 registers). The required registers are shown in Table 36. There is also an op-amp that must be biased. More details can be found in Section 4.11. The DC voltage level buffered by 2 op-amps can be observed on the external analog injection input pad. To do this, enable External analog injection, and Disable External digital injection.

Function	Register number	Register field	N. bits	Value
Vcal DAC bias	19	plsrDacBias	8	96
Vcal DAC setting	21	plsrDAC	10	0-1024
Current to voltage converter bias	14	BonnDAC	9	237
Delay current	17	PlsrIdacRamp	8	180
Delay value	31	PlsrDelay	6	0-63
Rise time	31	PlsrRiseUpTau	3	7
Enable	31	PlsrPwr	1	1
External digital	31	ExtDigCalSW	1	0
External analog	31	ExtAnaCalSW	1	0
Op-Amp bias	18	PlsrVgOPamp	8	255

**Table 36:** Configuration settings for internal pulser operation.

### 8.3 Stop Mode

Stop mode freezes all the latency counters for any pending hits on the chip, but allows TOT counters to finish recording the hit's charge (to be checked). This allows the read out of all hits stored in the array for all latency counter values. No new hits will be stored while in stop mode. In order to enter this mode, enable StopModeCnfg and return the chip to Rum Mode. As usual, sending a trigger will now initiate the readout of all regions that have a latency counter at the programmed latency value. The difference is that the region latency values are now stopped, so sending repeated triggers (or setting the trigger multiplier to greater than 1), will repeatedly read the same regions and the same data over and over. In order to read all data in all regions, sending triggers must be alternated with advancing the latency counters by one unit. To advance the latency counters, set StopClkPulse high and issue a Global Pulse. Alternatively, one can leave alone the latency counters and change the programmed latency value in between sending triggers. The latter method requires

re-entering run mode every time before sending the next trigger, whereas the former does not, since  
 1895 the global pulse command works in run mode.

#### 8.4 HitOr\_P(105)

HitOr\_P(105) is a convenient signal, available at the pad level, which is high whenever a pixel  
 comparator is high. The comparator of each pixel in a column is ORed together to form a HitBus.  
 The HitBus for a column is then ORed together with its column pair to form a double-column  
 1900 HitBus. Finally, each double-column HitBus is ORed together to form HitOr\_P(105). Inclusion  
 of a given pixel in HitOr\_P(105) is controlled by an enable bit in latch 8 of of the 13 pixel latches  
 (Table 26).

#### 8.5 Self Trigger

The user is also able to allow the HitBus signal to act as an input to the command decoder for  
 1905 “automatic” triggering. This is achieved by an enable bit called GateHitOr in global memory  
 register 27 (Appendix D). When this functionality is enabled, the HitBus signal going high will tell  
 the command decoder to issue a trigger pulse.

#### 8.6 HitLd

HitLd is a configuration bit which the user is able to control in Global Register 21. When this is  
 1910 enabled, a hit (small or big) will load a 1 into the shift register cell corresponding to that pixel. First  
 clear all the shift registers in the chip before enabling this function. To read out the data for a par-  
 ticular double-column first place the shift register in normal operating mode ( $S0=S1=HitLd=0$ ) and  
 issue a WrFrontEnd command to shift out the data. After processing the data the only information  
 which is received is whether or not a hit was registered in each pixel.

1915 **9. Output Data Format**

The FE-I4 runs from an externally supplied clock, nominally 40MHz. A clock multiplier inside the chip is used to be able to output data at the required rate of 160Mb/s. The default output mode is 8b/10b encoded, but this encoding can be switched off. 8b/10b encoding allows recovery of the 160 MHz clock from the data stream in the BOC/ROD in the control room and provides data framing and phase alignment. The data stream before encoding follows a few guidelines to facilitate data recognition when 8b/10b coding is turned off for testing purposes. The FE-I4 output is always sending out bits, which will be codes for idle output when there is no other output.

1920 **9.1 8b/10b**

Code Group	kin/kout	8-bit data	10-bit data (RD-)	10-bit data (RD+)
		HGF EDCBA	abcdei fghj	abcdei fghj
K28.0	1	000 11100	001111 0100	110000 1011
K28.1	1	001 11100	001111 1001	110000 0110
K28.2	1	010 11100	001111 0101	110000 1010
K28.3	1	011 11100	001111 0011	110000 1100
K28.4	1	100 11100	001111 0010	110000 1101
K28.5	1	101 11100	001111 1010	110000 0101
K28.6	1	110 11100	001111 0110	110000 1001
K28.7	1	111 11100	001111 1000	110000 0111
K23.7	1	111 10111	111010 1000	000101 0111
K27.7	1	111 11011	110110 1000	001001 0111
K29.7	1	111 11101	101110 1000	010001 0111
K30.7	1	111 11110	011110 1000	100001 0111

**Table 37:** The 12 commands, “K”-Code Group. On the two right columns, the two versions of actual 10b streams.

Many introductions to 8b/10b coding can be found in the literature [5, 2, 1]. An 8b/10b coder maps the 256 possible “symbols” of an 8-bit word into a specific subset of the 1024 symbols possible for a 10-bit word. The circuit that performs the mapping is called the coder. The selected 10b symbols have some favorable engineering properties:

- Each 10b word is either perfectly DC-balanced, or has a disparity of +2 or -2. The disparity of a word is defined as the number of 1’s minus the number of 0’s.
- There is always perfect DC balance over 20 bits. The coder keeps track of DC balance by evaluating a running disparity and compensates for positive or negative disparity with the next word sent.

- The coder can also generate 12 symbols which have a special meaning, in that they are decoded as commands. These commands are shown in Table 37. These symbols do not have an 8b representation, they only are possible after the 10b encoding.

1935

Of particular interest are the three commands K.28.1, K.28.5 and K.28.7. These three commands contain the unique stream 00.11111 (or the complementary stream 11.00000). This pattern can then be used for frame alignment, and these three commands are consequently called commas. The K.28.7 command cannot be generated from any single bit flip in the data stream. Conversely, a single bit flip in K.28.7 will result in K.28.1, K.28.5, or an undefined symbol. This is the only command which satisfies these single bit flip tolerance properties. However, no two K.28.7 can be used in a row or false codes can result in case of wrong synchronization.

1940

## 9.2 FE-I4 Protocol

The format used is based on a Start of Frame (SOF) using K.28.7, followed by 30 bit word(s) and an End of Frame (EOF) using K.28.5. Each 30-bit word corresponds to a 24-bit record before encoding. the protocol also has an Idle State based on K.28.1. the 24-bit records can be Data Header, Data Record, Address Record, Value Record, or Service Record. Detailed information about the various records is given later. When 8b/10b encoding is turned off, there is also a 24-bit Empty Record, which is transmitted whenever there is no other data (since the Idle State only exists after encoding).

1945

1950

**Idle State** When no records are pending to be transmitted, the Data Output Block takes care of keeping the output line busy with an Idle State consisting of K.28.1 commas. When 8b/10b is turned off for test purposes, Empty Records are transmitted instead.

**SOF** The Start of Frame is K.28.7. The purpose of K.28.7 is to provide a unique 1-bit flip tolerant stream that marks the beginning of the transmission of an event, and can be used for frame synchronization (see below). After a SOF, valid record words are Data Header, Address Record, Value Record, or Service Record. Data Record word(s) might only be present after a Data Header word. A triggered empty event is recognized by the absence of any Data Records after a Data Header. Value Record word(s) might be present after an Address Record word or also directly after an SOF (a read back mode where no address is read back).

1955

1960

**EOF** The End of Frame consists of one K.28.5 comma. The main purpose of the EOF is to provide some uniqueness in the stream between 2 events, which can then be used for frame synchronization during heavy data transmission when there may be no Idle States.

**Frame synchronization** Synchronization at the receiving hardware can be done by searching for a combination of two successive commas. The useful combinations for alignment are EOF followed by SOF, Idle State followed by SOF, or two consecutive Idle States (a total of six unique bit patterns when including code changes due to running disparity value).

1965

## 9.3 Records

Records are always described *unformatted*, meaning *before* 8b/10b encoding. All records are 24 bits long, divided into three 8-bit fields. All records except the Data Record and the Empty Record

1970

start with the pattern 11101, to ease the recognition of the start of transmission when 8b/10b is turned off. The six record types are summarized in Table 38) and a more detailed description follows, with bit order notation [MSB:LSB] and bit 0 comes out of the chip last in the serial stream.

**Data Header (DH)** | 11101 | 001 | Flag | [4:0]LV1ID | [9:0]bcID |

1975 *The header for transmission of pixel data*

- 11101: Eases the recognition of the start of transmission; tolerant to 1-bit flips.
- 001: Unique code for Data Header; 1-bit flip gives invalid code.
- Flag to indicate that errors have been logged.

1980 4:0 LV1ID: Value of the LV1ID counter. It counts trigger commands and has 12 bits. 5 bits are sent out in the DH, the remaining 7 MSB are sent in a special service record 14 when their value changes. The counter wraps around.

1985 9:0 BCID: Value of a counter of clock cycles received at the time of the trigger pulse for the given event. The BCID counter has 13 bits. 10 bits are sent out in the DH, the remaining 3 MSB are sent out in a special service record 14 when their value changes. The counter wraps around. Note that for a single trigger command received, up to 16 consecutive internal trigger pulses might be generated depending on the configuration. Each of these trigger pulses will result in a data header with the same LV1ID, but different BCID.

**Data Record (DR)** | [6:0]Column | [8:0]Row | [3:0]ToT(1) | [3:0]ToT(2) |

1990 *The pixel data*

6:0 Column: Column ID in binary. Numbering goes from 0000001 to 1010000.

8:0 Row: Row ID in binary. Numbering goes from 000000001 to 101010000.

3:0 ToT(1): ToT value for pixel (col,row).

3:0 ToT(2): ToT value for pixel (col,row+1).

1995 The pixel data sent out will be formatted using dynamic  $\phi$ -pairing, where a single Data Record is used to send information from two neighbor pixels adjacent inside the same column. The ToT value is itself a code and not exactly a ToT number. The meaning of the ToT code is given by Table 7. Whenever pixel 336 is hit but 335 is not, then dynamic  $\phi$ -pairing will assign row number 336, and the ToT(2) value (normally corresponding to row+1) will be 1111 (the code for no hit). See Figure 4. In general, when a record contains data for only one pixel, it will always be in the ToT(1) field with ToT(2)=1111. The ToT(1) field can never be 1111 (except due to an SEU upset): the combination ToT(1)=1111, ToT(2)=xxxx is not valid. After Data Record of a group the chip will send an Empty Record if 8b/10b is turned off.

2000

2005 **Address Record (AR)** | 11101 | 010 | Type | [14:0]Address |

*The address of a global register, or the position of the shift register*

- 11101: Eases the recognition of the start of transmission; tolerant to 1-bit flips.

- 010: Flags the Address Record; 1-bit flip gives invalid code.
- Type: 1-bit information. 0 identifies Global Register; 1 identifies Shift Register.

2010 14:0 Address: If Type is Global Register, address gives the Global Register ID. If Type is Shift Register, address gives the Shift Register position.

**Value Record (VR)** | 11101 | 100 | [15:0]Value |

*The value of a global register, or the value contained in the shift register*

- 11101: Eases the recognition of the start of transmission; tolerant to 1-bit flips.
- 100: Flags the Value Record; 1-bit flip gives invalid code.

2015

15:0 Value: Configuration read-back value.

Note that the use of 11101 followed by 100 for a Value Record allows also for sending Value Records with no Address Record in front.

**Service Record (SR)** | 11101 | 111 | [5:0]Code, [9:0]Counter |

2020

*A service message (e.g. error message, or extra information)*

- 11101: Eases the recognition of the start of transmission; tolerant to 1-bit flips.
- 111: Flags the Service Record; 1-bit flip gives invalid code.

5:0 Code: Message code (0-31). Codes are given in in Sec 9.5.

9:0 Payload: See Sec 9.5.

2025

**Empty Record (ER)** | abcdefgh abcdefgh abcdefgh |

When 8b/10b coding is turned off, to ease the recognition of the end of a data stream and to control the data output when nothing is pending to be sent out, 24-bit long Empty Records are constantly produced. The 8-bit pattern abcdefgh is programmable (normally it will simply be left at the default value of 00000000). One Empty Record will be sent after every group of Data Records belonging to the same Data Header. In 8b/10b mode the idle state is the K.28.1 comma the abcdefgh pattern is not used.

2030

**Precedence:** A Data Header, potentially followed by Data Record(s) and a single Service Record, has precedence over Configuration Read-Back (Address Record followed by Value Record(s) or directly Value Record(s)) which has precedence over Service Record(s). As long as no Data / Configuration / Service message needs to be transmitted, the Data Output Block will take care of transmitting Idle States (or Empty Records if 8b/10b is off). From the Idle State, as soon as Data or Configuration or Service message needs transmission, the Data Output Block will finish the transmission of the current K.28.1 comma (or Empty Record) and proceed with the transmission of relevant information. Note that Service Records are never transmitted by themselves unless there is a command requesting them. Spontaneous chip errors will result in an unrequested Service Record only after the next Data Header.

2040

24-bit Record Word	Field 1	Field 2	Field 3	Field 4	Field 5
Data Header DH	11101	001	Flag	LV1ID [4:0]	bcID [9:0]
Data Record DR	Column [6:0]	Row [8:0]	ToT(1) [3:0]	TOT(2) [3:0]	
Address Record AR	11101	010	Type	Address [14:0]	
Value Record VR	11101	100	Value [15:0]		
Service Record SR	11101	111	Code [5:0]	Number [9:0]	
Empty Record ER	abcdefgh	abcdefgh	abcdefgh		

**Table 38:** The Six 24-bit Record Words. The AR type is 0 to indicate that it is a Global Register address or 1 to indicate Shift Register position.

#### 9.4 Valid Record Sequences

There are only five valid sequences that records can follow. They are shown below both before (raw mode) and after 8b/10b encoding (framed) using the acronyms of Table 38:

1. Pixel Data:  
raw:  $(1) \times \text{DH}, (0/3) \times \text{SR}(14-16), (0/n) \times \text{DR}, (0/1) \times \text{SR}(\text{not } 14-16), (1) \times \text{ER}$   
framed: SOF,  $(1) \times \text{DH}, (0/3) \times \text{SR}(14-16), (0/n) \times \text{DR}, (0/1) \times \text{SR}(\text{not } 14-16), \text{EOF}$
2. Configuration with address read back:  
raw:  $(1/n) \times (\text{AR}, \text{VR})$   
framed: SOF,  $(1/n) \times (\text{AR}, \text{VR}), \text{EOF}$
3. Configuration with no address read back:  
raw:  $(1/n) \times \text{VR}$   
framed: SOF,  $(1/n) \times \text{VR}, \text{EOF}$
4. Read service records:  
raw:  $(31) \times \text{SR}$   
framed: SOF,  $(31) \times \text{SR}, \text{EOF}$
5. Idle:  
raw:  $(1/n) \times \text{ER}$   
framed:  $(1/n) \times \text{Idle}$

### 9.5 Service Record Details

The list of implemented service records in FE-I4B is given in Table ???. All service records begin with the bit pattern 11101111 followed by the 6-bit service code and the 10-bit payload (there are only 32 implemented codes even though the service record code is a 6-bit field). For all codes except 14, 15 and 16, the payload is the value of a dedicated 10-bit “error” counter. Each error counter simply counts input pulses coming from a block as indicated in the table. Whenever a service record is output, the corresponding counter is reset. If a service record is masked off, only the automatic output is masked off, but the corresponding counter will still count, and the final value can be interrogated with the read service records global pulse. All counters stop if they reach their maximum value- they do not warp around. For codes 14-16 the payload has a different specific meaning, as follows:

- 14: The payload is LV1Id[11:5], BC[12:10]
- 15: The payload is Skipped[9:0]
- 16: The payload is TF, ETC[4:0], L1Req [3:0], where TF is a truncated flag indicating if an event has been truncated. This will be 0 until an event is truncated and then always 1 until an Event Counter Reset is issued. ETC is the event truncation counter, which will count the number of events that have been truncated. L1req is the value of the internal L1 Request counter, which is normally not known to the user, but in this case will allow the user to identify when the value an request counter corresponding to a truncated event occurs again.

Code	Type	Meaning	From Block
0	ERR	BCID counter error	EOCHL
1	ERR	Hamming code error in word 0	EOCHL
2	ERR	Hamming code error in word 1	EOCHL
3	ERR	Hamming code error in word 2	EOCHL
4	ERR	L1_in counter error	EOCHL
5	ERR	L1 request counter error	EOCHL
6	ERR	L1 register error	EOCHL
7	ERR	L1 Trigger ID error	EOCHL
8	ERR	readout processor error	EOCHL
9	inf	Fifo_Full flag pulsed	EOCHL
10	inf	HitOr bus pulsed	Pixel Array
11-13		not used	
14	inf	3 MSBs of bunch counter and 7 MSBs of L1A counter	EOCHL
15	inf	Skipped trigger counter	EOCHL
16	inf	Truncated event flag and counter	EOCHL
17-20		not used	
21	inf	Reset bar RA2b pulsed	Pad, PRD <sup>1</sup>
22	inf	PLL generated clock phase faster than reference	CLKGEN
23	inf	Reference clock phase faster than PLL	CLKGEN
24	ERR	Triple redundant mismatch	CNFGMEM
25	ERR	Write register data error	CMD
26	ERR	Address error	CMD
27	ERR	Other command decoder error- see CMD section	CMD
28	inf	Bit flip detected in command decoder input stream	CMD
29	ERR	SEU upset detected in command decoder (triple redundant mismatch)	CMD
30	ERR	Data bus address error	DatabusMux
31	ERR	Triple redundant mismatch	EFUSE

1: Prompt Radiation Detector

**Table 39:** FE-I4B Service Record Codes

2080 **References**

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2090 **A. Complete List of Changes from FE-I4A to FE-I4B**

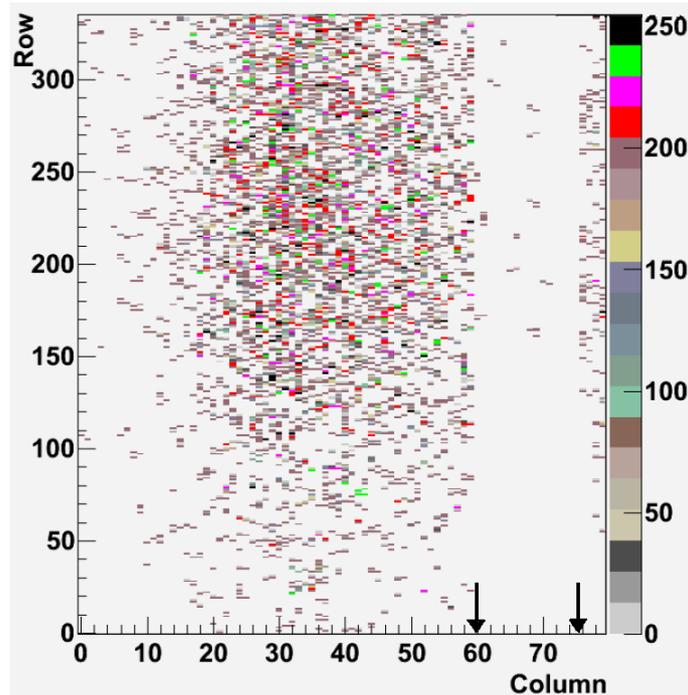
**A.1 Pixel Array**

- Used default metal capacitors in all columns (no VNCAPs). No difference in performance could be found.
- Used CPPM SEU latch design in all columns. SEU tests have shown these latches to have superior tolerance. At the same time, we have searched for performance issues with the CPPM latches, for example increased current during write or read, and have not found any. Fig. 50 shows a latch upset map from a recent PS exposure. This map was produced by disabling all pixel and then periodically injection charge during exposure. An upset from 0 to 1 of the pixel enable bit (one latch per pixel) will cause a pixel to respond to charge injection and show up in the plot.
- Used default comparator in all columns. The comparator has been carefully characterized, including absolute delay measurements vs. bias current and performs well at all temperatures. The contribution to the total chip current is Small enough that using the alternate, less well characterized design to try to save power is not justified.
- Changed injection capacitor switches to LP transistors to reduce leakage current to ground in switch off state. This will reduce the leakage current that the calibration pulser must overcome, extending the dynamic range. In FE-I4A the leakage current in the pixel array charge injection significantly limits the performance of the injection circuit. As a consequence, calibration after irradiation is only possible one column at a time, and even before irradiation linearity suffers if injecting to more than one column. the LP transistor leakage is at least 1 order of magnitude smaller than the presently used switches. The real value will have to be measured.
- Added output buffers to the nodes show in int Table 40 of the first pixel in the indicated columns. The buffer is active only for the column selected but the column pair address register, regardless of column pair mode. The buffers go to the analog MUX output. If none of the buffered columns is selected the analog MUX output is pulled low.

Column	Signal
to be completed	

**Table 40:** Signals monitored by the analog MUX circuit

- Added logic to disable S0 and S1 bits for columns that are not selected. This avoids a high current state in latch read-back mode caused by all latch outputs off leading to a floating inverter input. In FE-I4A the high current occurs in columns that are not selected when the S0 and S1 bits are set to high.



**Figure 50:** Latch upset map in PS run. Range of columns with CPPM type latches is indicated by the arrows.

## A.2 Injection Pulser

- Decreased output resistor value from 100K to 40K. This helps increasing the dynamic range but was not enough by itself without the change to LP transistors mentioned above.

## A.3 Bias Generator

2125 Changes are listed in Table 41. The PrmpVbp bias was scaled times 0.83, and additionally a safety *governor* bit has been added to the MSB, such that, unless the governor bit is set to 1, the ADC value will be given by the 7 LSBs only, regardless of the MSB in the configuration register. This prevents an accidental high current state. The governor bit is in the Efuse block.

## A.4 Configuration Memory and Efuse

- 2130
- Corrected reset polarity of Efuse- now reset-bar (reset-bar bit is in IOMux)
  - Added PrmpVbp MSB governor bit to Efuse
  - Efuse current reference trim bits (and voltage reference trim bits) no longer used.
  - New and changed configuration registers are listed in Table 42
- 2135
- Made CNFGMEM latch write logic triple redundant for all words except word 0. Word 0 is not used for anything (can write and read value for SEU testing). This was done following SEU test results showing that a coherent flipping of the 3 latches for a triple redundant bit was much bigger than expected from the individual upset rate of single SEU latches.

A COMPLETE LIST OF CHANGES FROM FE-I4A TO FE-I4B

Bias	Change	Reason / comment
PrmpVbp	$\times 0.83 \times 0.5$	Prevent accidental high current. See text
PrmpVbp_L	-	
PrmpVbp_R	-	
PrmpVbp_T	-	Not used
PrmpVbnFol	-	
PrmpVbpf	$\times 1.465$	hitting the 255 limit in FE-I4A
PrmpVbnLcc	-	
Amp2Vbn	-	
Amp2Vbp	-	
Amp2VbpFol	-	
Amp2Vbpf	-	
Vthin	bias eliminated	DAC reused for BufVgOpamp
VthinAlt_Coarse	$\times 0.5$	Make coverage continuous
VthinAlt_Fine	-	
DisVbn	-	
DisVbn_CPPM	bias eliminated	DAC reused for other purpose
TdacVbp	$\times 2$	hitting the 255 limit in FE-I4A
FdacVbn	$\times 0.5$	Setting $< 20$ in FE-IA for effective tuning
PlsrDacBias	-	
BonnDac	name eliminated	bias used for GADC Op Amp
PlsrDAC	-	
PlsrDelay	-	
PlsrdacRamp	$\times 2$	To reach 1 ns step size with margin
PlsrRiseUpTau	-	
PlsrVgOPamp	-	
LvdsDrvIref	-	
LvdsDrvVos	-	
lvdsDrvSet12	-	
lvdsDrvSet30	-	
lvdsDrvSet06	-	
PlIbias	-	
PlIcp	-	
TempSensIbias	Put to use	new TempSens block
VDDDtrim	New	Adjust digital ShuLDO voltage
VDDAtrim	New	Adjust analog ShuLDO voltage
BufVgOpamp	New	Bias for analog mux buffer Op Amp
GADCOpamp	New	Bias for generic ADC Op Amp

**Table 41:** List of bias modifications form FE-I4A to FE-I4B.

Register name	Deleted/Added	Register number/bits	Type
Vthin	Deleted	Reg 5 <0:7>	R/W
IREF trim	Deleted	Reg 34 <3:0>	R/W
Skipped_Triggers	Deleted	Reg 41	R-only
Read skipped pulse enable	Deleted	Reg 27 <11>	R/W
configBit <sup>1</sup>	Deleted	Reg 4 <6>	R/W
TempSensIbias	Enabled	Reg 16 <8:15>	R/W
GADC output	Enabled	Reg 40	R-only
GADC input select	Added	Reg 31 <0:2>	R/W
GADC enable and GADC start pulse	Added	Reg 27 <10>	R/W
Tempsens diode bias select	Added	Reg 30 <15:14>	R/W
Tempsens disable	Added	Reg 30 <13>	R/W
Monleak_range	Added	Reg 30 <12>	R/W
BufVgOpAmp	Added	Reg 5 <0:7>	R/W
VDDD trim	Added	check	R/W
VDDA trim	Added	check	R/W
AnaMux_Opamp	Added	check	R/W
Event_limit	Added	Reg 1 <0:7>	R/W
Duplicate_small_hit_suppression	Added	Reg 1 <8>	R/W
SR_readback_setup	Added	check	R/W

**Table 42:** Configuration registers deleted or added. In many cases the same register number is listed as deleted and added. This is to make it clear that the original function is no longer present and the bits have been taken over for a different function. <sup>1</sup>This bit was “overloaded” with 2 functions. It now has only one function that is ErrorMask<22>. The removed function was a phase adjustment for SR readback.

### A.5 End of Chip Logic

- 2140 • Eliminated error counters 14, 15, 16, 17 and 18 to make room for new functionality. Some of these addresses taken over for other functions (below).
- Increased Bunch Counter from 8 to 13 bits. 10 LSB bits come out in the new Data Header, with remaining 3 MSB bits in new service record 14.
- Increased LV1Id Counter from 7 bits to 12 bits. 5 LSB bits come out in the new Data Header, with remaining 7 MSB bits in new service record 14.
- 2145 • New Service Record 14 will come out under 2 conditions: increase of the 3 MSB of the Bunch Counter, or increase of the 7 MSB of the LV1Id counter. SR14 format 11101111, 001110, LV1Id[11:10], LV1Id[9:5], BC[12:10].
- New Data Header format: 11101001, SRFlag, LV1Id[4:0], BC[9:8], BC[7:0]

## A COMPLETE LIST OF CHANGES FROM FE-I4A TO FE-I4B

- 2150 • The ReadErrorRequest command has the added function of performing an ECR when the not in RunMode. This permits resetting the EOCHL and digital array before entering Run Mode so that no random garbage comes out.
- 2155 • Skipped Trigger Counter has been repaired (did not count in FE-I4A). It is also increased from 8 to 10 bits. It is read out in new Service Record 15, which comes out if there are skipped triggers. The skipped\_trigger read only register is no longer active. SR15 is 11101111, 001111, Skipped[9:8], Skipped[7:0]
- The Error Mask bits of Error Counters 14, 15 and 16 will continue to function to mask the output of these new service records. These new service records will come out when ReadErrorReq is issued regardless of the mask bits.
- 2160 • Event size limit function added. A 12 bit Event Size Counter (ESC) has been added, which counts write cycles to the FIFO. The 8 MSB of this counter are compared to the 8-bit Event Limit register. When the ESC[11:4] = EventLimit[7:0] the readout of this event will be ended. The system will continue with the next L1Req. Also, Service Record 16 will be sent out. The TF bit in SR16 is the truncated flag. It is set the first time an Event is truncated. SR16 will be sent out after the all Data Headers following a truncated event, until the next ECR. SR16 11101111, 010000, TF, ETC[4], ETC[3:0], L1Req [3:0]. ErrorMask[16]=1 can be used to disable SR 16 from coming out automatically, but the event size limit will still be in effect. Making the Event Limit 0 will disable the Event limiter.
- 2165
- 2170 • The newService Records 14, 15 and 16 are no longer part of the error block but part of the ReadOutController. In the ReadOutProcessor Some extra stages are added to send these records out between the Header and the Data. These special records come out with a new priority 16, 14, 15 and all 3 come out after one data header if all conditions occur. No other service records can follow in the same event if one of these comes out.
- 2175 • Added logic to suppress duplicate small hits generated in pixel array. Duplicate small hits occur naturally when two large hits happen in the same region separated by one bunch crossing- this is a feature of the region logic. The new suppression logic can be enabled/disabled with a new configuration bit
- 2180 • Changed circuit to pack shift register bits into data records. New circuit works for all phase relationships between shift register clock and EOCHL clock. The new circuit works for any arbitrary phase relationship between shift register clock and EOCHL clock, while the old circuit had a forbidden phase gap. A new register bit is added to setup SR readback by this new circuit. This setup must be done before each Write\_FE command to guarantee proper readback.

### A.6 Prompt Radiation Detector

2185 SEU tests showed that nuclear recoil events from high energy protons could fire both detectors in coincidence for any dose rate. The changes below will greatly increase tolerance to such single particle events, while the response to real high dose rate will be preserved. The increase of the

firing threshold will hopefully permit observation of the threshold in the Los Alamos proton beam, where the FE-I4A was seen to always fire even at the lowest available intensity.

- 2190 • Added a third copy of circuit and ANDed output with existing circuit number 2 (circuit number 1 is monitored with error counter).
- Increased threshold setting of all three from 1001 to 1111.

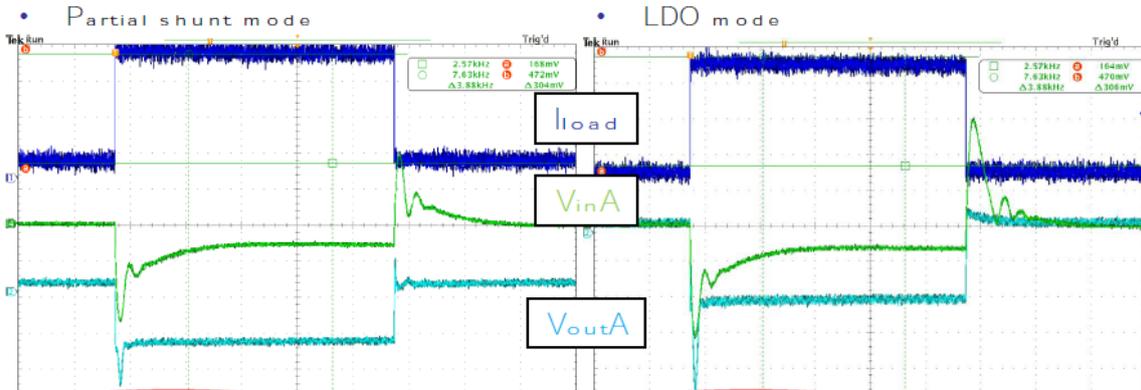
### A.7 Top Level

- 2195 • Changed routing of shift register output to EOCHL block. New circuit uses synchronization flip-flop to hold data while it is clocked into EOCHL. There is no longer a phase delay select bit.
- Added dedicated control of shift register readback setup. This is a configuration register bit that must be set before issuing a Write Front End command. Thus there a new Write Register command needed in the pixel configuration sequence.
- Internally connected Vthin\_C threshold setting.
- 2200 • Made connections to GADC inputs, including Monleak with a resistor to ground plus a new configuration range bit to shunt out part of this resistor.

### A.8 Power Circuits and Current Reference

- 2205 • Current reference trim bits adjusted to produce  $2\ \mu\text{A}$  in center of range. Bits now controlled by bond pads instead of Efuse bits. Pullup and pulldown resistors are included in these pads to produce  $2\ \mu\text{A}$  in nominal process if no bonds are made. This may minimize the need to make trim bonds on on each hybrid. Having the trim bits controlled by pads was the only safe option now that the current reference must be up at the correct value as soon as power is applied. This is because the regulator reference voltage is generated from the reference current.
- 2210 • Current reference now has 3 replicated outputs instead of 1. Two outputs are dedicated to generating reference voltages for ShuLDOs.
- Two bias DACs used to trim down the two reference voltages above.
- Current reference power now provided by analog ShuLDO output, with added startup circuit so that when current reference works when power is applied.
- 2215 • Rint bond pads eliminated from ShuLDOs and Rint node tied to VDDShunt pad. Rext pad still kept. This was done to make all needed pads standard width instead of narrow. Rext pad gives full flexibility- was not really needed to have Rint brought out to a pad.
- Internal shunt setting resistors changed from 2K to 8K in analog regulator and 16K in digital regulator. This gives approximately 160 mA of minimum current in the analog and 70 mA in the digital. The measured reduction of transients is shown in Fig. 51.
- 2220

- DC-DC charge pump has been removed. It was necessary to make room for new circuits and new bond pads.



**Figure 51:** Comparison of measured transients induced by changing load current on ShuLDO with partial shunt current (left) and in pure linear mode (right).

### A.9 Added Blocks

- Generic ADC. Selects 1 of 8 input voltages to digitize. The inputs 0-7 are: Tempsens, GADV Vref high, analog ground, output of analog MUX, voltage Vidd approximately equal to  $2\Omega$  times analog regulator current, 10 bit DAC output (input to the pulser), VDDA2/2, and Monleak into a resistor either 90K or 10K selectable by a range bit.
- Analog MUX. Selects analog voltages from bottom pixel from 1 of 8 columns and sends to an output pad at the chip bottom. This permits spying on various internal front end signals. The columns and signals are given in the AnaMUX section.
- Cap Measure. A charge pump controlled by Aux\_clk using as its capacitor a matrix of 1,000 pixel injection capacitors in the “11” value configuration. Has dedicated current input and output pins to be measured using an external device.
- Voltage reference. This is in addition to current reference to voltage converters described above. Use one or the other, not both.

### A.10 Wire Bond Pad Ring

- Changed SELCMD to pull up instead of pull down.
- Power for top of chip pads had been hard wired to VDDA2.
- Removed the following pads to make room for new functions and full width pads: PrmpVbp\_L (5), DisVbn\_CPPM (13), PrmpVbp\_R (15), Vthin\_P (16), Vref\_P (17), ILeak-Out\_P (23), Rint1\_P (121), CapBot\_P (126), CapTop\_P (127), DCDC\_IN (128), Rint2\_P (B6).

- 2245 • The following pads have been added: IleakOut, CrefVAAna, CrefVDig, VrefAna, VrefDig, AnaMuxOut, CapmeasureIn, CapmeasureOut, CrefTrim0, CrefTrim1, CrefTrim2, CrefTrim3, DetBias\_L2, DetBias\_R2.
- Current reference trim pads have internal pull-up and pull-down resistors to give  $2\ \mu\text{A}$  current in nominal process.
- All pads required for operation or wafer probing have been made full size instead of some of them narrow.
- 2250 • C-row pads for sensor bias ring bump pads have been split. There are now 4 C-row pads, one for each bias bump.

### A.11 Verification

All changed or new custom blocks have been checked with analog simulation including layout parasitics. The EOCHL has been verified with standalone simulation and formal timing analysis. 2255 Full chip simulations are described separately and have been carried out as if this were a new chip, not assuming features from FE-I4A still work in FE-I4B. The standalone analog simulations include:

- Injection pulser, including FEND injection switches.
- Pixel front end with the new LP injection switches and changed biases.
- 2260 • Bias DACs.
- Prompt radiation detectors.
- Generic ADC.
- Temperature sensor.
- Analog MUX.
- 2265 • Capmaesure circuit.
- ShuLDO + IREF + Startup + bias generation.
- CNFGMEM with new triplicated logic.

## B. Troubleshooting

This section lists some tips and tricks for troubleshooting FEI4\_A. No new information is presented here; only examples of practical methods to utilize functionality of the chip for debugging purposes. It is in general possible to test individual blocks without reliance on others in order to determine what is working and what is not. Scan chains are one useful method of testing the individual blocks, these scan chains do rely on the IOMUX to interface the data from the respective block.

The first step in troubleshooting is to eliminate mistakes in operating or configuring the chip. The following is a list of quick checks.

1. Power nets require multiple redundant connections. Use all or almost all the pads for each power net.
2. The LVDS output will not work until properly configured.
3. Readback of the pixel latches (13 per pixel) is the complement of their contents.
4. LSB/MSB order is not the same for all variables in the global memory registers.
5. The ToT values from hit data are encoded and not a straight number (see Table 7).
6. The latency counters count *down* from 255 to the Trig\_Lat, not up from 0 (see Section 8.1). Thus Trig\_Lat is not the actual latency.
7. Check that SelCmd\_P(85) is pulled high for normal chip operation.
8. The CLKGEN block must be configured properly (see Section 4.7 and Table 45).

### B.1 IOMUX

To check that a test system is working correctly, make use of the loopback mode of the IOMUX. This test will only depend on the IOMUX itself. By selecting the correct block (see Section 6.5) and providing a stimulus to the correct bond pad, the output is a slightly delayed copy of the input.

Another simple test using the IOMUX is to see if data is shifted properly through the abReg and cReg (as explained in Section 6.6)

### B.2 Command Decoder Operation

To check if the CMD is properly decoding commands look at IOMux outputs that directly originate in the CMD.

### B.3 Testing Downstream of the Command Decoder

To bypass the CMD, pulse Cmd\_ExtTrigger\_P(66) high for one clock cycle. External triggering is ORed together with the trigger output line of the command decoder, so pulsing this line has exactly the same effect as a successful trigger command. Furthermore this does not depend on the RunMode status of the chip. After the trigger the chip should output a data header (LV1ID and BCID) regardless if there was a hit or not. This test does rely on a large number of other blocks such as the DOB, EOCHL and CLKGEN.

**B.4 Alternate Configuration Register****B.5 Analog Outputs****B.6 Data Output Block and/or Clock Generator**

<sup>2305</sup> Setting `clk2OutCnfg` to 1 should present the DOB clock to its output. In order to avoid dependence on the CMD and configuration memory one program this bit using the alternative configuration register (see `SelAltBus_P(53)`). The DOB scan chain output (`DOBT_so`) will have the clock divided by 8 (10) for 8b/10b mode off (on), even while not running a scan chain test. This permits assessing indirectly at the CLKGEN and DOB operation even if the LVDS output is not functioning.

### 2310 C. Global Configuration Memory Map

Table 44 shows the bit assignments in the configuration memory, including the EFUSE block. This is an array of 16-bit words. Single bit functions are identified by a 3 character code and a dictionary of these codes is given Table 43. This section provides a hardware-oriented view of the chip configuration data. The same information is repeated in a function oriented view in Section D, 2315 ordered by field name, divided into initialization, options and functions, masks and values, and analog biases. In addition to the global memory there are read-only addresses that are only valid for the read register command:

- 40 Generic ADC output value
- 41 Event limit setting verification (redundant check of another register value)
- 2320 • 42 Internal error bits of CMD block (see CMD section)

All other 6-bit addresses are not valid and trying to read or write them will generate an error code (but will not have any adverse effect).

Code	Meaning	Code	Meaning
-	Not used	HLD	HITLD_IN shift register bit
40M	EN_40MHz	HOR	Gate_HitOR (prevents it from going to CMD)
80M	EN_80MHz	ILR	IleakRange
160	EN_160MHz	LEN	Latch_Enable control pulse enable
320	EN_320MHz	LV0	LVDSDrvSet06
ADC	GADCEn and GADCStart control pulse enable	LV1	LVDSDrvSet12
b7E	PrmpVbpMsbEn enables bit 7 of PrmpVbp	LV3	LVDSDrvSet30
c00	CLK0_S0	LVE	LVDSDrvEN
c01	CLK0_S1	N8b	no8b10bModeCnfg
c02	CLK0_S2	PLL	PLL_Enable bit
c10	CLK1_S0	PPW	PlsrPwr
c11	CLK1_S1	S0	Shift register mode bit S0
c12	CLK1_S2	S1	Shift register mode bit S1
c2o	Clk2OutCnfg	SMX	SmallHitErase
CAE	Conf_AddrEnable	SRC	SRClr control pulse enable
CAL	CalEn enable digital injection using global pulse	SRK	SR_Clock control pulse enable
CP0	Column pair mode bit 0	SRR	SRRread shift register read-back setup bit
CP1	Column pair mode bit 1	STC	StopModeCnfg
DHS	DIGHITIN_SEL	STP	StopClkPulse stop mode clock control pulse enable
DJO	DINJ_Override	TM0	TmpSensD0 diode bias sel 0
EFS	EFUSE_Sense control pulse enable	TM1	TmpSensD1 diode bias sel 1
HD0	HitDiscCnfg[0]	TMX	TmpSensDisable
HD1	HitDiscCnfg[1]	XAC	ExtAnaCalSW
		XDC	ExtDigCalSW

**Table 43:** Dictionary of 3 character bit codes from memory map

C GLOBAL CONFIGURATION MEMORY MAP

Register Address	Bit																
	Send F first in serial steam.....Send 0 last																
	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
0	spare																
1	-	-	-	-	-	-	-	SMX	EventLimit: MSB								
2	MSB: Trig_Count				CAE		spare										
3	ErrorMask_0 for service records 15-0																
4	ErrorMask_1 for service records 31-16																
5	PrmpVbp_R: MSB								MSB: BufVgOpAmp and GADCVref								
6	spare								PrmpVbp: MSB								
7	TDACVbp: MSB								DisVbn: MSB								
8	Amp2Vbn: MSB								Amp2VbpFol: MSB								
9	spare								Amp2Vbp: MSB								
10	FDACVbn: MSB								Amp2Vbpff: MSB								
11	PrmpVbnFol: MSB								PrmpVbp_L: MSB								
12	PrmpVbpf: MSB								PrmpVbnLCC: MSB								
13	S1	S0	Pixel latch strobe 0 to						Pixel latch strobe 12						-		
14	LVDSDrvIref: MSB								GADCCompBias: MSB								
15	PlIbIbias: MSB								LVDSDrvVos: MSB								
16	TempSensIbias: MSB								PlIcP: MSB								
17	spare								PlsrIDACRamp: MSB								
18	VrefDigTune: MSB								PlsrVgOpAmp: MSB								
19	PlsrDACbias: MSB								VrefAnTune: MSB								
20	Vthin_Coarse (global threshold): MSB								Vthin_Fine (global threshold): MSB								
21	-	-	-	HLD	DJO	DHS	PlsrDAC (calibration voltage): MSB										
22	-	-	-	-	-	-	CP0	CP1	Colpr_Addr: MSB						-	-	
23	DisableColCnfg0 disable bits for digital double columns 15-0																
24	DisableColCnfg1 disable bits for digital double columns 31-16																
25	MSB: Trig_Lat (trigger latency)								DisableColCnfg2 disable bits for DDC 39-32								
26	MSB: CMDcnt12 (bits 12-0 of 14 bits for CMD pulse settings, bit 13 is M13)												STC	HD1	HD0		
27	PLL	EFS	STP	RER	-	ADC	SRR	-	-	-	HOR	CAL	SRC	LEN	SRK	M13	
28	LV0	-	-	-	-	-	40M	80M	c10	c11	c12	c00	c01	c02	160	320	
29	-	-	N8b	c2o	EmptyRecordCnfg: MSB								-	LVE	LV3	LV1	
30	TM0	TM1	TMX	ILR													
31	PlsrRiseUpTau			PPW	PlsrDelay: MSB						XDC	XAC	-	MSB: GADCSel			
32	SELB(0:15) EFUSE bits to select B shift register for column pairs 15-0																
33	SELB(16-31) EFUSE bits to select B shift register for column pairs 31-16																
34	SELB(32-39) EFUSE SRB colpr 39-32								-	-	-	b7E	-	-	-	-	
35	EFUSE Serial number user bits (no function inside chip)																

**Table 44:** Map of global configuration memory, including CNFGMEM and EFUSE. The acronym “MSB” indicates the position of the most significant bit of a given word.

## D. Configuration Parameters

This appendix presents a different view of the configuration parameters than the global registers table, but it does not contain independent information. In general this list should be a more convenient place to look for a particular parameter or to have an overview of what parameters are available. This list does not give the internal position of bits within a given register - refer to Appendix C for the internal structure of each register.

### D.1 Initialization of the Chip

[2]	[1]	[0]	Selects
0	0	0	RefCLK (input clock to chip)
0	0	1	F320M (320 MHz)
0	1	0	RefCLK (input clock to chip)
0	1	1	F320M (320 MHz)
1	0	0	F160M (160 MHz)
1	0	1	F80M (80 MHz)
1	1	0	F40M (40 MHz regenerated clock)
1	1	1	AuxCLK (auxiliary input to chip)

**Table 45:** Multiplexer Selection for CLK0 and CLK1 of the CLKGEN Block

#### 2330 EN\_PLL

Size: 1-bit Controls: CLKGEN Suggested value: 1

Global Register: 27 Alternate Register: C[79]

Enables the CLKGEN block to produce clock output.

#### CLK0

2335 Size: 3-bit Controls: CLKGEN Suggested value: 100 (binary)

Global Register: 28 Alternate Register: C[82:84]

Control bit for CLK0 multiplexer output. Clock0 controls the DOB. See Table 45.

#### CLK1

Size: 3-bit Controls: CLKGEN Suggested value: 000 or 110 (binary)

2340 Global Register: 28 Alternate Register: C[85:87]

Control bit for CLK1 multiplexer output. Clock1 controls everything else except for the CMD and DOB. See Table 45.

#### EN\_320M

Size: 1-bit Controls: CLKGEN Suggested value: 0

2345 Global Register: 28 Alternate Register: C[80]

Enables the 320 MHz clock inside CLKGEN block. Note that the clock still has to be selected in one of the CLKGEN muxes.

**EN\_160M**

Size: 1-bit Controls: CLKGEN Suggested value: 1

2350 Global Register: 28 Alternate Register: C[81]

Enables the 160 MHz clock inside CLKGEN block. Note that the clock still has to be selected in one of the CLKGEN muxes.

**EN\_80M**

Size: 1-bit Controls: CLKGEN Suggested value: 0

2355 Global Register: 28 Alternate Register: C[88]

Enables the 80 MHz clock inside the CLKGEN block. Note that the clock still has to be selected in one of the CLKGEN muxes.

**EN\_40M**

Size: 1-bit Controls: CLKGEN Suggested value: 1

2360 Global Register: 28 Alternate Register: C[89]

Enables the 40 MHz clock inside the CLKGEN block. Note that the clock still has to be selected in one of the CLKGEN muxes.

**LVDSDrvEN**

Size: 1-bit Controls: IOB Suggested value: 1

2365 Global Register: 29 Alternate Register: C[98]

This switches on the LVDS data output driver. The output will be tri-stated if this bit is off.

**GateHitOr**

Size: 1-bit Controls: CMD Suggested value: 0

Global Register: 27 Alternate Register: C[69]

2370 HitOr is a signal which is high whenever any enabled pixel comparators in the entire chip are high; all the comparator outputs are “ORed” together with HitOr being the output. When GateHitOr is enabled, this pulse is routed to the CMD to produce a self-trigger. The actual trigger happens 16 clocks after the HitOr pulse to allow for ToT to complete. Note that when this is enabled do not expect the Trigger ID, which is stored inside the data header, to be anything meaningful; make  
2375 sure to reset the Trigger ID after turning the self-trigger off to restore meaning to the counter when issuing trigger commands.

**DIGITIN\_SEL**

Size: 1-bit Controls: array Suggested value: 1

Global Register: 21 Alternate Register: AB[143]

2380 In addition to the procedure necessary to create digital hits in pixels with either a GlobalPulse or CAL command, this bit must also be set high since it is ANDed with the input pulse signals. A digital inject scan will not be possible with this bit low.

**PlsrPwr**

Size: 1-bit Controls: PULSEGEN Suggested value: 1

2385 Global Register: 31 Alternate Register: C[140]

This bit switches on the calibration pulse delay generator. If this bit is set low, one cannot use the calibration injection command to inject hits (analog or digital).

### VrefDigTune

Size: 8-bit Controls: ShuLDO Suggested value: TBD

2390 Global Register: 18 Alternate Register: AB[72:79]

Adjustment of digital ShuLDO voltage.

### VrefAnTune

Size: 8-bit Controls: ShuLDO Suggested value: TBD

Global Register: 19 Alternate Register: AB[80:87]

2395 Adjustment of analog ShuLDO voltage.

## D.2 Options / Functions

### Colpr\_Mode

Size: 2-bit Controls: array Suggested value: 0

Global Register: 22 Alternate Register: AB[128:129]

2400 When performing operations on the double-columns, these two bits determine what double-columns are affected relative to the addressed Colpr\_Addr. See Table 23.

### Colpr\_Addr

Size: 6-bit Controls: array Suggested value: 0-39

Global Register: 22 Alternate Register: AB[130:135]

2405 The address of the double-column for all double-column operations. Numbers zero through 39 correspond to the 40 double-columns on the chip. Numbers greater than 39 are valid for talking to column pairs in modes other than 00, but have special read-back meaning such as loop-back of the input. See Table 24.

### Conf\_AddrEnable

2410 Size: 1-bit Controls: EOCHL Suggested value: 1

Global Register: 2 Alternate Register: N/A

Enables the sending of an “address record” (in addition to “value record”) in response to a RdRegister command on any of the global memories. When this bit is enabled, the EOCHL places an address record before every value record in the data stream to be passed to the DOB.

2415 **no8b10b**

Size: 1-bit Controls: DOB Suggested value: 0

Global Register: 29 Alternate Register: C[109]

Disables 8b/10b encoding of the DOB data output.

### Clk2OutCnfg

2420 Size: 1-bit Controls: DOB Suggested value: 0

Global Register: 29     Alternate Register: C[108]

This is a select line for a 2-1 MUX which controls what is presented to the DOB output. If this bit is 0, the normal data is displayed. If this bit is 1, the input clock of the DOB is displayed. This is useful for debugging and for mark space ratio tuning of optical links.

#### 2425 **PxStrobes**

Size: 13-bit     Controls: FEND     Suggested value: 0

Global Register: 13     Alternate Register: AB[274:286]

2430 Enable line for each of the 13 strobes for the pixel latches. If high, when a GlobalPulse is issued with LatchEn enabled and S0=S1=0, the shift register cell value will be loaded into the corresponding pixel latch(es). The strobes are also used to select which latch to read back into the shift register. See Table 26.

#### **S0**

Size: 1-bit     Controls: FEND     Suggested value: 0

Global Register: 13     Alternate Register: AB[273]

2435 Controls the input to the double-column shift registers. See Table 25.

#### **S1**

Size: 1-bit     Controls: FEND     Suggested value: 0

Global Register: 13     Alternate Register: AB[272]

Controls the input to the double-column shift registers. See Table 25.

#### 2440 **HITLD\_IN**

Size: 1-bit     Controls: FEND     Suggested value: 0

Global Register: 21     Alternate Register: AB[141]

2445 If this bit is enabled, a pixel hit will load a 1 into the corresponding shift register cell. This could then be read out by setting HITLD\_IN=0, ensuring S0=S1=0 and reading out the shift register. See Table 25.

#### **DINJ\_Override**

Size: 1-bit     Controls: array     Suggested value: 0

Global Register: 21     Alternate Register: AB[142]

2450 This is a way to set the digital injection line to always high. This is provided for testing the pixel digital regions in stop mode. For expert use only.

#### **StopModeCnfg**

Size: 1-bit     Controls: EODCL     Suggested value: 0

Global Register: 26     Alternate Register: C[50]

2455 If this bit is high, stop mode is enabled. Stop mode freezes all the latency counters for any pending hits in the chip. This allows to read out all hits stored in the array for all latency counter values, but no new hits will be stored while in stop mode. This is a very useful mode for testing the digital region.

**ExtAnaCalSW**

Size: 1-bit Controls: PULSEGEN, IOB Suggested value: 0

2460 Global Register: 31 Alternate Register: C[132]

This enables external analog charge injection from the dedicated input pad.

**ExtDigCalSW**

Size: 1-bit Controls: PULSEGEN, IOB Suggested value: 0

Global Register: 31 Alternate Register: C[133]

2465 This enables external digital injection from the dedicated input pad.

**SRRead**

Size: 1-bit Controls: EOCHL Suggested value: 0

Global Register: 27 Alternate Register: C[73]

2470 This bit must be pulsed to set up the end of chip logic to receive and pack pixel shift register bits into data records for output. Set bit high before each WriteFrontEnd command.

**GADCsel**

Size: 3-bit Controls: GADC Suggested value: 0-7

Global Register: 31 Alternate Register: C[130:128]

Selection bits to define the GADC output. See Table 12.

2475 **TempSensDiodeBiasSel**

Size: 2-bit Controls: TempSens Suggested value: TBD

Global Register: 30 Alternate Register: C[126:127]

**TempSensDisable**

2480 Size: 1-bit Controls: TempSens Suggested value: 0

Global Register: 30 Alternate Register: C[125]

Set this bit to disable the TempSens block.

**MonleakRange**

Size: 1-bit Controls: Suggested value: 0

2485 Global Register: 30 Alternate Register: C[124]

Adjustment of range for monitoring leakage current.

**D.3 Digital Value Settings and Masks****Trig\_Count**

Size: 4-bit Controls: EOCHL Suggested value: 1

2490 Global Register: 2 Alternate Register: N/A

Number of consecutive triggers to send upon issue of trigger command. After the CMD decodes the command, it is sent to the EOCHL where it is then multiplied. This is useful for trigger scans

since the trigger command itself takes 5 clock cycles to issue. If there were no multiplier, the most often you could trigger would be every 5 clock cycles. Value 0000 means 16 consecutive triggers.

#### 2495 **Trig\_Lat**

Size: 8-bit Controls: EOCHL Suggested value: 0-254

Global Register: 25 Alternate Register: C[40:47]

8-Bit complement of trigger latency in clock cycles (true latency = 255 - Trig\_Lat). When a hit is registered in a pixel, a latency counter starts counting up from the programmed Trig\_Lat value in the corresponding PDR. When the counter reaches 255, the hit will be erased unless a trigger was issued. Events which have their latency counter equal to 255 when a trigger is present will be flagged for readout. Do not program the value Trig\_Lat = 255.

#### **EventLimit**

Size: 8-bit Controls: EOCHL Suggested value: 0-255

2505 Global Register: 1 Alternate Register: N/A

This bit allows to limit the event size. A counter in the EOCHL counts the write pulses to the FIFO. The 8 MSB of this counter are compared to the EventLimit setting. If the counter exceeds the EventLimit the readout will be ended. EventLimit=1 corresponds to a limit of 16 events, EventLimit=0 disables the event limiter.

#### 2510 **CMDcnt**

Size: 14-bit Controls: CMD Suggested value: 0

Global Register: 26 Alternate Register: C[51:64]

These bits control the CAL pulse for internal analog or digital injection.

2515 CMDcnt[13:8] sets the delay, in clock cycle units, between the command detection and the beginning of the pulse. All values 0-63 are allowed.

CMDcnt[7:0] instead sets the width, always in clock cycles, of the CAL pulse that will be generated. The possible range is any value 0-255 resulting in pulse width 1-256 clocks.

#### **HitDiscCnfg**

Size: 2-bit Controls: EODCL, PDR Suggested value: 2

2520 Global Register: 26 Alternate Register: C[48:49]

These two bits discriminate between “small” and “big” hits in the PDRs. Pulse widths less than or equal to HitDiscCnfg are considered small, while hits larger than it are considered big. Do not use a value of 2'b11 = 2'd3.

#### **SmallHitErase**

2525 Size: 1-bit Controls: EOCHL Suggested value: 0

Global Register: 1 Alternate Register: N/A

If this bit is set hits with ToT=14 ("small" hits) will not be sent to the readout. This bit has been added to suppress duplicated small hits (see appendix A).

#### **ErrorMask**

2530 Size: 32-bit Controls: EOCHL Suggested value: 0

Global Register: 3, 4     Alternate Register: N/A

There are 32 error counters/lines in the chip. When errors in the chip are detected a service request is automatically flagged to be sent out for that particular error code. This service record itself will come out after the next data header is requested/sent and its counter reset. If the corresponding bit  
 2535 is enabled in ErrorMask, the chip will completely neglect sending out the service request automatically for that error. If a Rd\_ErrorRequest pulse is sent to the EOCHL, all the error counters are sent to the user and then reset, regardless of the mask settings.

### **SELB**

Size: 40-bit     Controls: array     Suggested value: 0

2540 Global Register: 32, 33, 34     Alternate Register: N/A

Each of the 40 double-columns has a shift register associated with it. If one of these shift registers becomes corrupt the user has the option of using a spare shift register which can be enabled by setting high the corresponding bit in SELB. Note that this configuration can be copied to the EFUSE so that it is loaded by default upon chip power up. Also note that this B backup shift register does  
 2545 not have latch read back capability - it can only be used to program the pixel latches but not to read them back.

### **DisableColCnfg**

Size: 40-bit     Controls: EODCL     Suggested value: 0

Global Register: 23, 24, 25     Alternate Register: C[0:39]

2550 Setting a particular bit high will completely disable the digital portion of the selected double-column.

### **Chip\_SN**

Size: 16-bit     Controls: N/A     Suggested value: 0-65535

Global Register: 35     Alternate Register: N/A

2555 This is the chip serial number. Note that this configuration can be copied to the EFUSE to permanently burn in a serial number.

### **EmptyRecordCnfg**

Size: 8-bit     Controls: DOB     Suggested value: 0

Global Register: 29     Alternate Register: C[100:107]

2560 The DOB sends out empty records when the EOCHL FIFO is empty. If no8b10b is enabled (i.e. the DOB does not encode the output data), then the DOB uses this word as its “comma” instead of the 8b/10b K.28.1.

## **D.4 Control Pulser**

All bits in this section are useful only in conjunction with a GlobalPulse command. They simply  
 2565 enable possible destinations for the global pulse. Any of them can be enabled simultaneously.

### **SR\_Clock**

Size: 1-bit     Controls: CTRLPULSER, EOCHL     Suggested value: N/A

Global Register: 27     Alternate Register: C[65]

If this bit is high when a GlobalPulse is issued, a single clock pulse is sent to the SR\_Clock input in the EOCHL.

### LatchEn

Size: 1-bit     Controls: CTRLPULSER     Suggested value: N/A

Global Register: 27     Alternate Register: C[66]

If this bit is high when a GlobalPulse is issued, the value in the shift register cell will be copied into the pixel latches which are selected in PxStrobes. This applies to the double-columns which are selected via Colpr\_Addr and Colpr\_Mode.

### SRClr

Size: 1-bit     Controls: CTRLPULSER     Suggested value: N/A

Global Register: 27     Alternate Register: C[67]

If this bit is high when a GlobalPulse is issued, the double-column shift registers which are selected (i.e. Colpr\_Mode and Colpr\_Addr) will be all set to zero.

### CalEn

Size: 1-bit     Controls: CTRLPULSER     Suggested value: N/A

Global Register: 27     Alternate Register: C[68]

Having this bit enabled allows a GlobalPulse command to essentially act as a CalibrationPulse command with digital injection enabled. Please note that DIGHITIN\_SEL must also be enabled for this to work. The width of the pulse (which affects the ToT values) is adjusted by sending different width GlobalPulse commands.

### ReadErrorReq

Size: 1-bit     Controls: CTRLPULSER, EOCHL     Suggested value: N/A

Global Register: 27     Alternate Register: C[76]

If this bit is high when a GlobalPulse is issued, the EOCHL will send out a “service record” for all 32 error lines (regardless of the value of ERRORMASK). After the service records are sent out, the counters are also cleared.

### StopClkPulse

Size: 1-bit     Controls: CTRLPULSER     Suggested value: N/A

Global Register: 27     Alternate Register: C[77]

If this bit is high when a GlobalPulse is issued and the chip is in stop mode (i.e StopModeCnfg is enabled), trigger latency counters for pixels which have registered hits will be incremented by one.

### EFUSE\_Sense

Size: 1-bit     Controls: CTRLPULSER, EFUSE     Suggested value: N/A

Global Register: 27     Alternate Register: C[78]

If this bit is high when a GlobalPulse is issued, the EFUSE registers will be reloaded with their PROM values. Anything the user has written to those registers will be lost.

2605 **GADCStart**

Size: 1-bit Controls: CTRLPULSER, GADC Suggested value: N/A

Global Register: 27 Alternate Register: C[74]

If this bit is high when a GlobalPulse is issued, the pulse will be sent to the GADC and the value of the selected channel will be written to GR 40. GADCStart is also the inverse of GADCDisable.

2610 **D.5 Analog Biases**

Please note that the global memory register and alternate shift register positions of the analog settings have not been verified in the SystemVerilog test bench.

**PrmpVbp**

Size: 8-bit Controls: Columns 2-39 Input transistor current Suggested value:

2615 43

Global Register: 6 Alternate Register: AB[160:167]

Main preamp bias. This setting will have the greatest impact on the VDDA2 current of the chip. Set to 00 to turn off the preamps and most of the current.

**PrmpVbp\_L**

2620 Size: 8-bit Controls: Column 1 Input transistor current Suggested value: 43

Global Register: 11 Alternate Register: AB[240:247]

This controls only the pixels in column 1 and is provided in case of long pixels.

**PrmpVbp\_R**

Size: 8-bit Controls: Column 40 Input transistor current Suggested value: 43

2625 Global Register: 5 Alternate Register: AB[152:159]

This controls only the pixels in column 40 and is provided in case of long pixels.

**PrmpVbnFol**

Size: 8-bit Controls: Preamp follower bias Suggested value: 106

Global Register: 11 Alternate Register: AB[248:255]

2630 Bias to the follower of the first stage. This follower drives the coupling capacitor between first and second stages.

**PrmpVbpf**

Size: 8-bit Controls: Preamp feedback Suggested value: 20

Global Register: 12 Alternate Register: AB[264:271]

2635 This is the master feedback current of the preamp. It sets the fall time of preamp output which in turn determines the ToT LSB scale. There is a 4-bit trim of this current in each pixel.

**PrmpVbnLcc**

Size: 8-bit Controls: Preamp leakage compensation Suggested value: 0

Global Register: 12 Alternate Register: AB[256:263]

2640 Leakage current compensation circuit bias.

**Amp2Vbn**

Size: 8-bit Controls: Second stage main bias Suggested value: 79

Global Register: 8 Alternate Register: AB[200:207]

2645 **Amp2Vbp**

Size: 8-bit Controls: Second stage load bias Suggested value: 85

Global Register: 9 Alternate Register: AB[208:215]

**Amp2VbpFol**

2650 Size: 8-bit Controls: Second stage follower bias Suggested value: 26

Global Register: 8 Alternate Register: AB[192:199]

**Amp2Vbpff**

Size: 8-bit Controls: Second stage feedback current Suggested value: 50

2655 Global Register: 10 Alternate Register: AB[224:231]

Feedback current for second stage amplifier. This is bias is the most sensitive to radiation in the front end. In early test chip prototypes it was discovered that the second stage could stop working after irradiation even at the maximum setting for this bias. For the full size FE-I4 the bias range was increased. The suggested value of 50 is needed after 250 Mrad based on FE-I4A irradiation results.

2660 Unirradiated much lower values (down to 10) will work, but also 50 is fine before irradiation.

**Vthin\_Fine/Vthin\_Coarse**

Size: 16-bit Controls: Vthin\_C output voltage Suggested value: N/A

Global Register: 20 Alternate Register: AB[96:111]

Two 8 bit values for coarse and fine threshold adjustment. The coarse scale is non-linear. Range is 0 to 1V.

2665

**DisVbn**

Size: 8-bit Controls: Discriminator bias for baseline columns Suggested value: 26

Global Register: 7 Alternate Register: AB[176:183]

2670 Discriminator bias.

**TdacVbp**

Size: 8-bit Controls: TDAC LSB size Suggested value: 255

Global Register: 7 Alternate Register: AB[184:191]

Sets the step size (LSB) of the in-pixel threshold tuning 5-bit DAC.

2675 **FdacVbn**

Size: 8-bit Controls: FDAC LSB size Suggested value: 50

Global Register: 10 Alternate Register: AB[232:239]

Sets the step size (LSB) for the in-pixel amplifier feedback current DAC.

### **GADCVref**

2680 Size: 8-bit    Controls: GADC    Suggested value: n/a  
Global Register: 5    Alternate Register:  
see BufVgOpAmp and GADCVref.

### **GADCCompBias**

2685 Size: 8-bit    Controls: GADC    Suggested value: 100  
Global Register: 14    Alternate Register: AB[0:7]  
Bias for GADC comparator.

### **PlsrDacBias**

2690 Size: 8-bit    Controls:    Suggested value: 96  
Global Register: 19    Alternate Register: AB[88:95]  
Bias for calibration voltage DAC.

### **PlsrDAC**

Size: 10-bit    Controls: PULSER    Suggested value: 0-1023  
Global Register: 21    Alternate Register: AB[112:121]  
Calibration injection voltage value (VCAL).

### 2695 **PlsrDelay**

Size: 6-bit    Controls: PULSER    Suggested value: 2  
Global Register: 31    Alternate Register: C[134:139]  
Analog fine delay value for the calibration pulse. Applies to both digital and analog injection. This delay is added on top of the CMDcnt delay.

### 2700 **PlsrlacRamp**

Size: 8-bit    Controls: PULSER    Suggested value: 180  
Global Register: 17    Alternate Register: AB[48:55]  
This is the bias current for the analog delay generator above. It controls the delay step size. It can also be used to adjust the delay, but the delay is proportional to the inverse of this current, while the PlsrDelay adjustment is linear. See Fig. 32.

### 2710 **PlsrRiseUpTau**

Size: 3-bit    Controls: PULSER    Suggested value: 7  
Global Register: 31    Alternate Register: C[141:143]  
Sets the speed of the return to baseline of the analog calibration pulse. The baseline is the VCAL voltage (see PlsrDAC). To inject charge the voltage is switched very fast from baseline to ground and held at ground for the duration of the CAL pulse (see CMDcnt). After this time the voltage linearly ramps back up to VCAL to avoid reverse polarity injection. The speed of this ramp is controlled by this bias.

**PlsrVgOPamp**

2715 Size: 8-bit Controls: PULSER Suggested value: 255

Global Register: 18 Alternate Register: AB[64:71]

Bias for op-amps used in pulse generator.

**BufVgOpAmp and GADCVref**

Size: 8-bit Controls: ANA\_MUX Suggested value: 50

2720 Global Register: 5 Alternate Register: AB[144:151]

This bias has two outputs a positive output that controls GADCVref and an inverted output that controls BufVgOpAmp. GADCVref is the reference voltage for generic ADC. The ADC compares the input to be digitized to this voltage for the MSB, to half this voltage for the next bit, etc. The bias setting is actually a current that is sourced onto an internal resistor to generate the reference voltage.

2725 It should be set close to maximum to have a good dynamic range of the ADC. BufVgOpAmp is the Bias for op-amps of analog mux buffer. The buffer acts on the bottom pixel of the selected column. It is active for only one column at a time (selected by the ColPr\_Addr). This bias wants to be greater than 0.7. Unfortunately, the inverted output means that 0 setting gives maximum bias. Thus it seems impossible to choose a setting that achieves both a high value of GADCVref and BufVgOpAmp above 0.7 V. It is therefore suggested to override GADCVref with VDDDD from outside (nominally 1.2 V) which leaves the bias setting dedicated to BufVgOpAmp (hence the suggested value of 50).

2730

**LVDSDrvIref**

Size: 8-bit Controls: LVDS driver bias current Suggested value: 171

2735 Global Register: 14 Alternate Register: AB[8:15]

**LVDSDrvVos**

Size: 8-bit Controls: LVDS driver offset voltage Suggested value: 105

Global Register: 15 Alternate Register: AB[16:23]

2740

**LVDSDrvSet12**

Size: 1-bit Controls: LVDS driver strength Suggested value: 1

Global Register: 29 Alternate Register: C[96]

Coarse control of the output current of the LVDS output.

2745 **LVDSDrvSet30**

Size: 1-bit Controls: LVDS driver strength Suggested value: 1

Global Register: 29 Alternate Register: C[97]

Medium control of the output current of the LVDS output.

**LVDSDrvSet06**

2750 Size: 1-bit Controls: LVDS driver strength Suggested value: 1

Global Register: 28 Alternate Register: C[95]

Fine control of the output current of the LVDS output.

**PLLbias**

Size: 8-bit    Controls: PLL bias current    Suggested value: 88

2755 Global Register: 15    Alternate Register: AB[24:31]

Bias current of PLL oscillator

**PLLcp**

Size: 8-bit    Controls: PLL comparator bias    Suggested value: 28

Global Register: 16    Alternate Register: AB[32:39]

2760 Bias current of comparator in PLL phase detector

**TempSensIbias**

Size: 8-bit    Controls: TempSens    Suggested value: TBD

Global Register: 16    Alternate Register: AB[40:47]

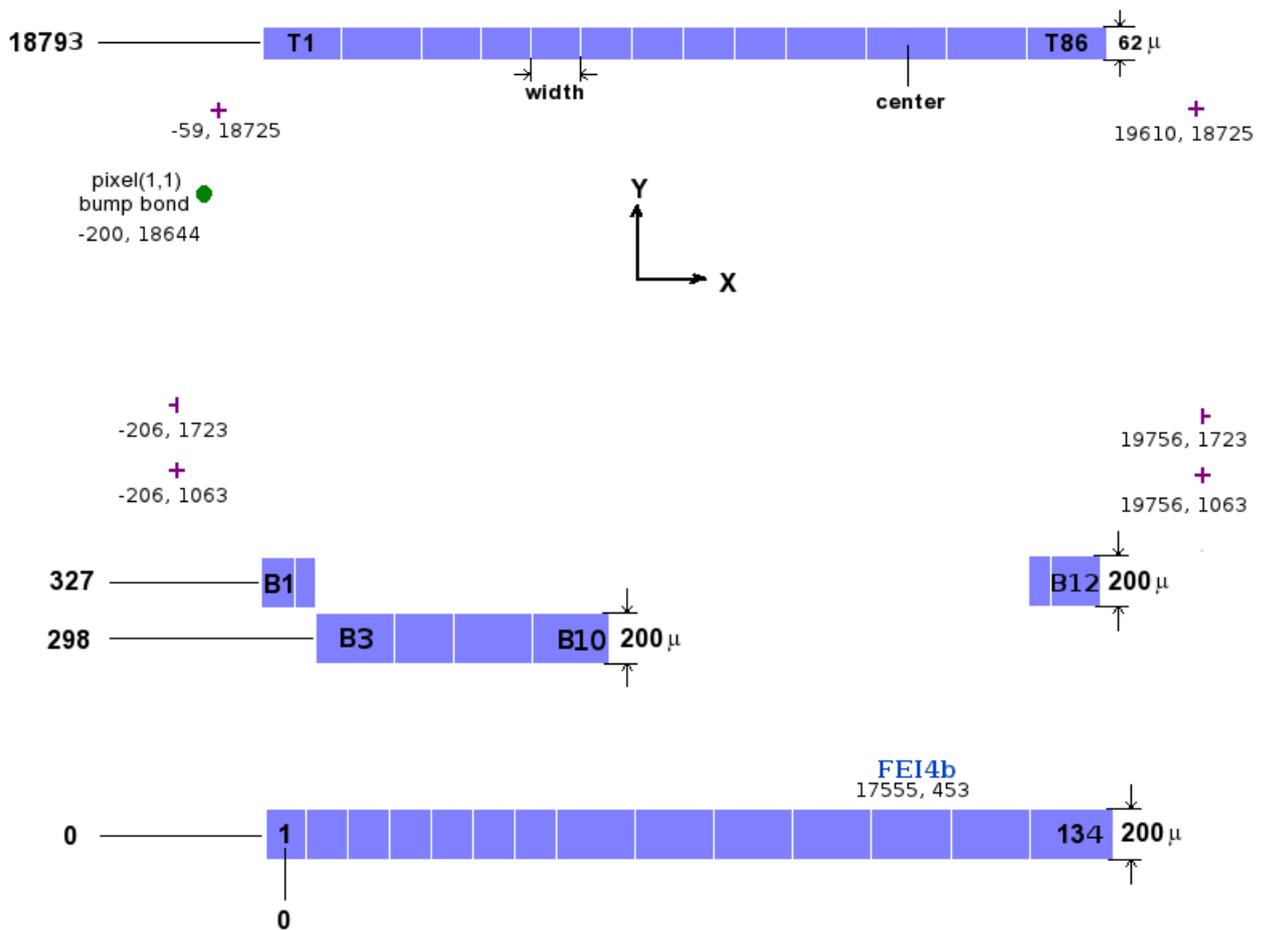
Bias for the temperature sensor.

2765 **E. Alternate configuration**

The FE-I4 has a kind of “safe mode” configuration option that allows limited operation of the pixel array without making use of the command decoder or the global configuration memory. This is based on a simple shift register serial input of all global configuration bits, as well as direct control of some needed internal signals.

2770 **F. Wire Bond Pads**

Fig. 52 shows the layout of the wire bond pads and alignment marks. Table 46 gives the list of the bond pads on the front row of pads along the chip bottom, Table 47 for the back (inner) row of pads along the chip bottom, and Table 48 gives the list for the top row of pads. The bottom front and back row pads are 200  $\mu\text{m}$  high, the top row pads are 62  $\mu\text{m}$  high. The vertical coordinate for each row of pads is given in Fig. 52, while the horizontal coordinate for each pad can be found in the tables. All coordinates are given relative to the center of the glass opening for pad 1. The coordinates of the alignment marks, bump pad center for pixel (1,1), and FEI4b logo are also shown in Fig. 52. The tables show what each pad should be connected to for normal IBL detector use.



**Figure 52:** Layout of wire bond pads, alignment marks, pixel (1,1) bump pad, and logo. Not to scale. All coordinates are in microns relative to the center of the glass opening for pad 1. The coordinates given for the FEI4b logo refer to the center of the letter I.

Pad Num	Name	Center ( $\mu\text{m}$ )	Wid ( $\mu\text{m}$ )	Description	Connect to in IBL
1	AnOut_P	0	100	Buffered preamp out pixel 1/336. Needs 1 k $\Omega$ pullup.	
2	PrmpVbpf_P	130	75	Main preamp feedback bias access	
3	PrmpVbnLcc_P	230	75	Leakage compensation amp bias access	
4	PrmpVbnFol_P	330	75	Preamp follower bias access	
5	IleakOut_P	430	75	Pixel leakage current sum monitor	
6	FdacVbn_P	530	75	LSB of the preamp feedback DAC access	
7	Amp2Vbpf_P	630	75	Second stage feedback bias access	
8	Amp2Vbp_P	730	75	Second stage load bias access	
9	Amp2Vbn_P	830	75	Second stage main bias access	
10	Amp2VbpFol_P	930	75	Second stage follower bias access	
11	TdacVbp_P	1030	75	LSB of the pixel threshold DAC access	
12	DisVbn_P	1130	75	Discriminator bias access	
13	PrmpVbp_P	1230	75	Preamp main bias for columns 2-79 access	
14	PlIbias_P	1330	75	Clock multiplier PLL main bias access	
15	VrefOutAn_P	1467	100	Adjustable reference voltage A derived from current reference	B8 Vref2_P <sup>(1)</sup>
16	PlIcp_P	1617	100	Clock multiplier PLL charge pump bias access	
17	LvdsDrvIref_P	1767	100	LVDS driver main bias access	
18	LvdsDrvVos_P	1917	100	LVDS driver common mode offset access	
19	BgVrefAn_P	2067	100	Fixed reference voltage of 0.75V from voltage reference	B8 Vref2_P <sup>(1)</sup>
20	VthinC_P	2217	100	Global threshold voltage access	
21	VrefOutDig_P	2367	100	Adjustable reference voltage D derived from current reference	117 Vref1 <sup>(2)</sup>
22	GND A2	2525	100	Analog ground	ground
23	VSS	2675	100	Substrate	ground
24	VDD A2	2825	100	Analog power for array and biases	B4 REG2_OUT
25	VDD D2	2975	100	Digital power for EOCHL, DDC, etc.	120 REG1_OUT
26	GND D2	3125	100	Digital ground	ground
27	VSS	3275	100	Substrate	ground
28	VDD T3_Shield	3425	100	Internal shield tied to T3 n-wells	B4 REG2_OUT
29	Iref_out_P	3575	100	Output reference current of 2 $\mu\text{A}$ (after trimming)	30 VbbnIn_P
30	VbbnIn_P	3725	100	Master reference current input for bias generator	29 Iref_out_P
31	GND A2	3875	100	Analog ground	ground
32	VDD A2	4025	100	Analog power for array and biases	B4 REG2_OUT

Continued on next page

Table 46 – continued from previous page

Pad Num	Name	Center (μm)	Wid (μm)	Description	Connect to in IBL
33	GNDA2	4175	100	Analog ground	ground
34	VDDA2	4325	100	Analog power for array and biases	B4 REG2_OUT
35	VDDD2	4475	100	Digital power for EOCHL, DDC, etc.	120 REG1_OUT
36	GNDD2	4625	100	Digital ground	ground
37	VDD33	4775	100	3.3V input for Efuse programming	
38	VDDEfuse	4925	100	Power input of Efuse circuit	B4 REG2_OUT
39	VDDA1	5075	100	analog power for CNFGMEM, etc.	B4 REG2_OUT
40	GNDA1	5225	100	Analog ground	ground
41	RA1bar_P	5375	100	Analog reset-bar input (1 of 2)	
42	ExtAnaInjectIn	5525	100	External analog injection override input	
43	GadcVref_P	5675	100	Reference voltage for generic ADC	120 REG1_OUT
44	VDDA1	5825	100	analog power for CNFGMEM, etc.	B4 REG2_OUT
45	GNDA1	5975	100	Analog ground	ground
46	ExtDigInjectIn	6125	100	External digital injection override input	
47	regABStbld_P	6275	100	Alternative configuration register AB strobe load signal input	
48	regABDacld_P	6425	100	Alternative configuration register AB DAC load signal input	
49	SelAltBus_P	6575	100	Alternative configuration register enable input	
50	VDDA1	6725	100	analog power for CNFGMEM, etc.	B4 REG2_OUT
51	GNDA1	6875	100	Analog ground	ground
52	RA2bar_P	7025	100	Analog reset-bar input (2 of 2)	
53	GNDA2	7175	100	Analog ground	ground
54	VSS	7325	100	Substrate	ground
55	VDDA2	7475	100	Analog power for array and biases	B4 REG2_OUT
56	VDDD2	7625	100	Digital power for EOCHL, DDC, etc.	120 REG1_OUT
57	GNDD2	7775	100	Digital ground	ground
58	VSS	7925	100	Substrate	ground
59	VDDT3_Pad	8075	100	T3 n-wells	B4 REG2_OUT
60	VDDD1	8225	100	Digital power for CMD and LVDS	120 REG1_OUT
61	GNDD1	8375	100	Digital ground	ground
62	Cmd_ExtTrigger	8525	100	L1A Trigger override input	
63	Cmd_ChipId<0>	8675	100	Chip ID bit 0 input	VDDD1 to set
64	Cmd_ChipId<1>	8825	100	Chip ID bit 1 input	
65	Cmd_ChipId<2>	8963	75	Chip ID bit 2 input	
66	Cmd_AltPls_P	9100	100	Internal control pulse override input	
67	IoMxSel_P<2>	9250	100	I/O Mux address bit 2 input	

Continued on next page

Table 46 – continued from previous page

Pad Num	Name	Center (μm)	Wid (μm)	Description	Connect to in IBL
68	IoMxSel_P<1>	9400	100	I/O Mux address bit 1 input	
69	IoMxSel_P<0>	9550	100	I/O Mux address bit 0 input	
70	IoMxIn_P<0>	9700	100	I/O Mux data bit 0 input	
71	IoMxIn_P<1>	9850	100	I/O Mux data bit 1 input	
72	IoMxIn_P<2>	10000	100	I/O Mux data bit 2 input	
73	IoMxIn_P<3>	10150	100	I/O Mux data bit 3 input	
74	VDDD1	10300	100	Digital power for CMD, LVDS, I/O mux	120 REG1_OUT
75	GNDD1	10450	100	Digital ground	ground
76	VDD_PLL	10600	100	Digital power for clock multiplier PLL	120 REG1_OUT
77	GND_PLL	10750	100	Digital ground	ground
78	IoMxOut_P<0>	10900	100	I/O Mux ouptut 0	
79	IoMxOut_P<1>	11050	100	I/O Mux ouptut 1	
80	IoMxOut_P<2>	11200	100	I/O Mux ouptut 2	
81	SelCmd_P	11350	100	Command decoder enable (int. pull up)	
82	VDDD1	11500	100	Digital power for CMD, LVDS, I/O mux	120 REG1_OUT
83	GNDD1	11650	100	Digital ground	ground
84	RD1bar_P	11800	100	Command decoder reset bar	
85	RD2bar_P	11950	100	End of Chip Logic reset bar	
86	Aux_Clk_N	12100	100	Auxiliary clock differential inverting input	ground
87	Aux_Clk_P	12250	100	Auxiliary clock differential noninverting input	120 REG1_OUT
88	Ref_Clk_N	12400	100	Beam crossing clock inverting input	Clock-bar in
89	Ref_Clk_P	12550	100	Beam crossing clock noninverting input	Clock in
90	CMD_DCI_N	12700	100	Serial command differential inverting input	DCI-bar in
91	CMD_DCI_P	12850	100	Serial command differential noninverting input	DCI in
92	VDDD1	13000	100	Digital power for CMD, LVDS, I/O mux	120 REG1_OUT
93	GNDD1	13150	100	Digital ground	ground
94	LvdsRecVbn_P	13288	75	LVDS receiver bias access	
95	LvdsRecVbp_P	13388	75	LVDS receiver bias access	
96	GNDA2	13525	100	Analog ground	ground
97	VSS	13675	100	Substrate	ground
98	VDDA2	13825	100	Analog power for array and biases	B4 REG2_OUT
99	DOB_OUT_P	13975	100	Differential serial noninverting output	Data out
100	DOB_OUT_N	14125	100	Differential serial inverting output	Data out bar
101	HitOr_P	14275	100	Hit bus monitoring output	
102	VDDD2	14425	100	Digital power for EOCHL, DDC, etc.	120 REG1_OUT
103	GNDD2	14575	100	Digital ground	ground
104	VSS	14725	100	Substrate	ground

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Table 46 – continued from previous page

Pad Num	Name	Center (μm)	Wid (μm)	Description	Connect to in IBL
105	VDDT3_Pad	14875	100	T3 n-wells	B4 REG2_OUT
106	VDDD2	15025	100	Digital power for EOCHL, DDC, etc.	120 REG1_OUT
107	GNDD2	15175	100	Digital ground	ground
108	VDDD2	15325	100	Digital power for EOCHL, DDC, etc.	120 REG1_OUT
109	GNDD2	15475	100	Digital ground	ground
110	GNDA2	15625	100	Analog ground	ground
111	VDDA2	15775	100	Analog power for array and biases	B4 REG2_OUT
112	GNDA2	15925	100	Analog ground	ground
113	VDDA2	16075	100	Analog power for array and biases	B4 REG2_OUT
114	Vbp1_P	16212	75	Voltage reference bias access	
115	BgVrefDg_P	16312	75	Fixed reference voltage of 0.6V from voltage reference	117 Vref1 <sup>(2)</sup>
116	Rext1_P	16412	75	Digital regulator external shunt current setting resistor	
117	Vref1	16550	100	Digital regulator voltage reference input	21 or 115
118	VddShunt1	16700	100	Digital regulator shunt current enable	unreg. V in
119	REG1_GND	16925	250	Digital regulator ground	ground
120	REG1_OUT	17225	250	Digital regulator output	VDD1, VDD2, VDD_PLL
121	REG1_IN	17525	250	Digital regulator input	unreg. V in
122	IrefTune_P<3>	17750	100	Current reference trim bit 3 input	TBD by calib.
123	IrefTune_P<2>	17900	100	Current reference trim bit 2 input	TBD by calib.
124	IrefTune_P<1>	18050	100	Current reference trim bit 1 input	TBD by calib.
125	IrefTune_P<0>	18200	100	Current reference trim bit 0 input	TBD by calib.
126	CapMeasGnd	18350	100	Return current of cap measure test circuit	
127	CapMeasVin	18500	100	Supply current of cap measure test circuit	
128	GNDA2	18650	100	Analog ground	ground
129	VSS	18800	100	Substrate	ground
130	VDDA2	18950	100	Analog power for array and biases	B4 REG2_OUT
131	VDDD2	19100	100	Digital power for EOCHL, DDC, etc.	120 REG1_OUT
132	GNDD2	19250	100	Digital ground	ground
133	VSS	19400	100	Substrate	ground
134	VDDT3_Shield	19550	100	Internal shield tied to T3 n-wells	B4 REG2_OUT

**Table 46:** Front row of pads on chip bottom. Connections shown are for IBL modules, with blank meaning no connection. Inputs that do not require a connection have internal pull up or pull down resistors. <sup>(1)</sup>, <sup>(2)</sup>Connect one or the other but not both.

Pad Num	Name	Center ( $\mu\text{m}$ )	Wid. ( $\mu\text{m}$ )	Description	Connect to in IBL
B1	DetBias_L	-169	100	Contact to leftmost bump pad	
B2	DetBias_L2	59	100	Contact to 2 <sup>nd</sup> bump on left	
B3	REG2_IN	265	250	Analog regulator input	Unreg. V in
B4	REG2_OUT	565	250	Analog regulator output	VDDA1, VDDA2, VDD_efuse, T3, Shield
B5	REG2_GND	865	250	Analog regulator ground	ground
B6	VDDShunt2	1090	100	Analog regulator shunt current enable	Unreg. V in
B7	Rext2_P	1240	100	Analog regulator external shunt current setting resistor	
B8	Vref2_P	1390	100	Analog regulator voltage reference input	15 or 19, not both
B9	Vbp2_P	1540	100	Analog reference bias monitor/override	
B10	VSS	1690	100	Substrate	ground
B11	DetBias_R2	19336	100	Contact to 2 <sup>nd</sup> bump on right	
B12	DetBias_R	19719	100	Contact to rightmost bump pad	

**Table 47:** Back row of pads on chip bottom. Connections shown are for IBL modules, with blank meaning no connection.

Pad Num	Name	Center ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Description
T1	IleakOut	139	140	Pixel array leakage current monitoring bus
T2	InjectInL1	365	140	Access to calibration injection of column 1
T3	GNDA2M	591	140	Analog ground monitoring
T4	vtheEffL<1>	816	140	Access to global threshold voltage for column 1
T5	VDDA2M	1042	140	Analog power monitoring
T6	GNDD2M	1268	140	Analog ground monitoring
T7	VDDD2M	1493	140	Analog power monitoring
T8	outD2<0>	1719	140	Hit OR output of pix 1 col 1.
T9	outD1<0>	1945	140	Comparator output for pixel 1 column 1
T10	outD1<1>	2171	140	Comparator output for pixel 1 column 2
T11	outD2<1>	2396	140	Hit OR output of pix 1 col 2
T12	outD2<2>	2622	140	Hit OR output of pix 1 col 3
T13	outD1<2>	2848	140	Comparator output for pixel 1 column 3
T14	VDDD2	3074	140	Digital voltage (internally connected)
T15	GNDD2	3299	140	Digital ground

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Table 48 – continued from previous page

Pad Num	Name	Center ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Description
T16	GND A2	3525	140	Analog ground monitoring
T17	VDD A2	3751	140	Analog voltage (internally connected)
T18	out2<0>	3976	140	Buffered 2 <sup>nd</sup> stage output for pixel 1 column 1
T19	out1<0>	4202	140	Buffered preamp output of pix 1 col 1. Need external pullup.
T20	out1<1>	4428	140	Buffered preamp output of pix 1 col 2. Need external pullup.
T21	out2<1>	4654	140	Buffered 2 <sup>nd</sup> stage output for pix 1 col 2
T22	out2<2>	4879	140	Buffered 2 <sup>nd</sup> stage output for pix 1 col 3
T23	out1<2>	5105	140	Buffered preamp output of pix 1 col 3. Need external pullup.
T24	PwrEnable_L	5265	140	Left side analog Mux enable
T25	Sel_L<3>	5491	140	Left Mux select bit 3
T26	out_L<3>	5717	140	Left Mux output 3
T27	Vg_L	5942	140	Left Mux bias
T28	out_L<2>	6168	140	Left Mux output 2
T29	VSS	6394	140	Substrate
T30	out_L<1>	6619	140	Left Mux output 1
T31	GND A2	6845	140	Analog ground monitoring
T32	VDD A2	7071	140	Analog voltage (internally connected)
T33	out_L<0>	7297	140	Left Mux output 0
T34	Sel_L<2>	7522	140	Left Mux select bit 2
T35	Sel_L<1>	7748	140	Left Mux select bit 1
T36	Sel_L<0>	7974	140	Left Mux select bit 0
T37	PwrEnable	8265	140	Middle analog Mux enable
T38	Sel<3>	8491	140	Middle Mux select bit 3
T39	out<3>	8717	140	Middle Mux output 3
T40	Vg	8942	140	Middle Mux bias
T41	out<2>	9168	140	Middle Mux output 2
T42	VSS	9394	140	Substrate
T43	out<1>	9619	140	Middle Mux output 1
T44	GND A2	9845	140	Analog ground monitoring
T45	VDD A2	10071	140	Analog voltage (internally connected)
T46	out<0>	10297	140	Middle Mux output 0
T47	Sel<2>	10522	140	Middle Mux select bit 2
T48	Sel<1>	10748	140	Middle Mux select bit 1

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Table 48 – continued from previous page

Pad Num	Name	Center ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Description
T49	Sel<0>	10974	140	Middle Mux select bit 0
T50	PwrEnable_R	11265	140	Right analog Mux enable
T51	Sel_R<3>	11491	140	Right Mux select bit 3
T52	out_R<3>	11717	140	Right Mux output 3
T53	Vg_R	11942	140	Right Mux bias
T54	out_R<2>	12168	140	Right Mux output 2
T55	VSS	12394	140	Substrate
T56	out_R<1>	12619	140	Right Mux output 1
T57	GNDA2	12845	140	Analog ground monitoring
T58	VDDA2	13071	140	Analog voltage (internally connected)
T59	out_R<0>	13297	140	Right Mux output 0
T60	Sel_R<2>	13522	140	Right Mux select bit 2
T61	Sel_R<1>	13748	140	Right Mux select bit 1
T62	Sel_R<0>	13974	140	Right Mux select bit 0
T63	vbpBuf	14219	140	Bias for the simple analog buffers.
T64	out1_R<2>	14445	140	Buffered preamp output of pix 1 col 78. Need external pullup.
T65	out2_R<2>	14671	140	Buffered 2 <sup>nd</sup> stage output for pix 1 col 78
T66	out2_R<1>	14897	140	Buffered 2 <sup>nd</sup> stage output for pix 1 col 79
T67	out1_R<1>	15122	140	Buffered preamp output of pix 1 col 78. Need external pullup.
T68	out1_R<0>	15348	140	Buffered preamp output of pix 1 col 80. Need external pullup.
T69	out2_R<0>	15574	140	Buffered 2 <sup>nd</sup> stage output for pixel 1 column 80
T70	VDDA2	15799	140	Analog voltage (internally connected)
T71	GNDA2	16025	140	Analog ground monitoring
T72	GNDD2	16251	140	Digital ground
T73	VDDD2	16477	140	Digital voltage (internally connected)
T74	outD1_R<2>	16702	140	Comparator output for pixel 1 column 78
T75	outD2_R<2>	16928	140	Hit OR output of pix 1 col 78
T76	outD2_R<1>	17154	140	Hit OR output of pix 1 col 79
T77	outD1_R<1>	17380	140	Comparator output for pixel 1 column 79
T78	outD1_R<0>	17605	140	Comparator output for pixel 1 column 80
T79	outD2_R<0>	17831	140	Hit OR output of pix 1 col 80
T80	VDDD2M	18057	140	Digital voltage monitoring
T81	GNDD2M	18282	140	Digital ground monitoring

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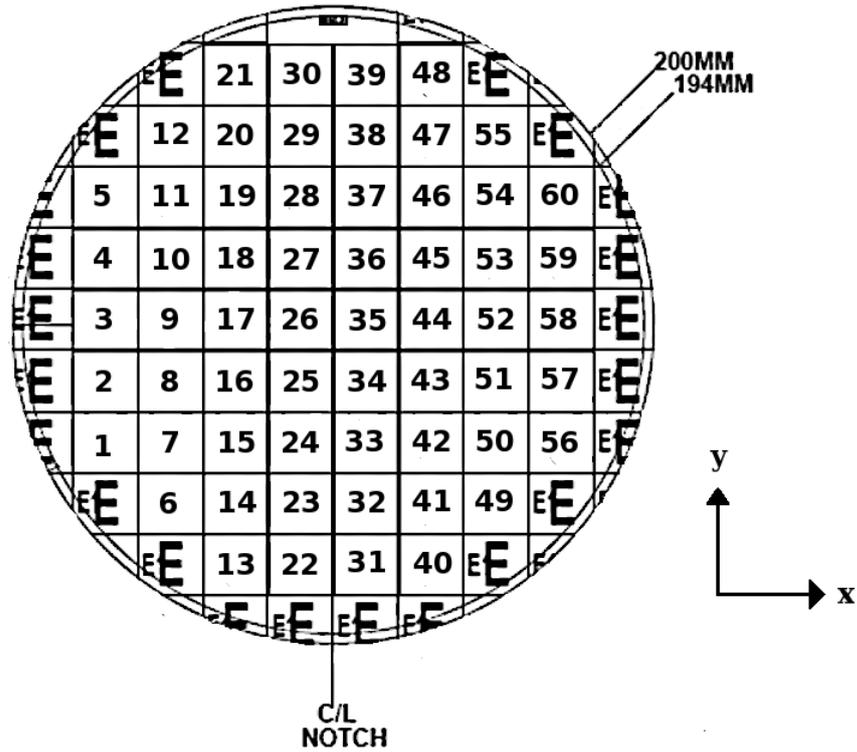
**Table 48 – continued from previous page**

<b>Pad Num</b>	<b>Name</b>	<b>Center (<math>\mu\text{m}</math>)</b>	<b>Width (<math>\mu\text{m}</math>)</b>	<b>Description</b>
T82	VDDA2M	18508	140	Analog ground monitoring
T83	vtheEffR<1>	18734	140	Access to global threshold voltage for column 80
T84	GND A2M	18960	140	Analog ground monitoring
T85	InjectInR40	19185	140	Access to calibration injection of column 80
T86	IleakOut	19411	140	Pixel array leakage current monitoring bus

**Table 48:** Top Row Pads. The ESD rail for these pads is VDDA\_T with GND A\_T.

**G. FE-I4B Wafer Information**

The FE-I4B chip is fabricated on 200 mm diameter wafers with 60 chips per wafer. The same wafer layout was preserved from FE-I4A to minimize setup changes for bump deposition, etc. Figure 53 shows the wafer layout along with the numbering of the chips. The stepping dimensions are given in Table 49. Although the crack stop is not active circuitry, it must not be removed during dicing as it is needed to protect the circuit from damage due to crack propagation.



**Figure 53:** Layout of the FE-I4B wafer, showing the numbering of the individual chips. Partial chips marked with the letter “E” are empty reticles not actually printed on the physical wafer. The coordinate origin is at the center of the wafer.

The 16-bit serial number to be programmed into the Efuse read only memory will contain the wafer number and chip number as shown in Table 50.

	x ( $\mu\text{m}$ )	y ( $\mu\text{m}$ )
<b>chip size</b>	20030.16	18962.56
<b>crack-stop</b>	15.00	15.00
<b>dicing road</b>	270.00	270.00
<b>chip to chip pitch</b>	20330.16	19262.56
<b>Chip 1 center</b>	-71156.24	-36943.64

**Table 49:** Dimensions of circuit and wafer stepping. The coordinate origin is at the center of the wafer.

<b>Bits [MSB-LSB]</b>	[15]	[14-6]	[5-0]
<b>Content</b>	reserved	wafer number	chip number

**Table 50:** Content of programmable read-only 16-bit serial number